Design of a Low-Power Broadband Monolithic Receiver Front-End for LTE Mobile Application Based on the 65-nm Bulk CMOS Process

1. Abstract:

Mobile multimedia services have quickly occupied the market, providing people with a better wireless communication experience. In order to carry multimedia services, demands for high speed and high-capacity communication such as real-time video streaming are increasing. Therefore a broadband, high-speed system that supports multi-types users and business integration is required. TD-LTE (known as 3.9G) has been developing rapidly to meet the demand. As the evolution of LTE technology, bandwidth and spatial dimensions has been increased in LTE-A standard, which is well compatible with LTE technology. A report about the demand of LTE-A technology was completed in June 2008, proposing the minimum requirements for LTE-A, 1 Gb/s for the downlink peak rate and 500 Mb/s for the uplink peak rate. The spectrum utilization is 15 bps/Hz for uplink and 30 bps/Hz for downlink. The design and implementation on radio frequency front-end for LTE-A base-station is the target of this project. The transceiver operates at 2600 MHZ with 100MHz bandwidth. The linear output power is 0.2W according to the standard. The control range of both the transmitter and receiver are 60dB.

2. Target Group:

This work should be a graduation project for the 4th grade of the Electronics & Communications Engineering (ECE) department in Fayoum University. A group of 2 to 4 students may apply. The students should have a good electronics as well as Microwave background and find them interesting. They will learn more on the RF Front-End architectures, RF design specifications, IC design issues including layout and physical verification. Using cadence efficiently for simulations with PVT and corners analysis is one of the important goals of this project.

3. Methodology:

A theoretical background will be firstly built, through either lecturing or self-study or both, from a well-known commonly used text books such as [1] and [2]. And tutorials of the cadence tool and the necessary simulation techniques will always be self-studied from day one. In the second part of the project you will start reading papers to select the TRx topology and design your own. The supervisor will convey his experience in the RFIC design and guide them to select the appropriate topologies of the TRx building blocks and extract results from the test benches.

4. Outcome:

a. Experienced students with the RFIC design to compete with others in the Egyptian Electronics and IC job market.
b. Ready for fabrication transmitter and receiver on the TSMC 65-nm CMOS.
c. A well written paper with a state-of-the-art results to be published in one of the international periodical or conference.

5. Time Plan:

Stage	Period (10 Months Project)
1st stage: Literature Review	Sep. – Nov.
2nd stage: System planning, Blocks simulations	Dec. – Mar.
3rd stage: Layout, LVS, DRC, Post-layout Simulation	Apr. – Jun.

6. References:

[1] Thomas H. Lee, ”The Design of CMOS Radio Frequency Integrated Circuits”
[2] Behzad Razavi, “RF Microelectronics”

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