New CMOS Fully-Differential Transconductor and Application to a Fully-Differential Gm-C Filter

Mohamed O. Shaker, Soliman A. Mahmoud, and Ahmed M. Soliman

A new CMOS voltage-controlled fully-differential transconductor is presented. The basic structure of the proposed transconductor is based on a four-MOS transistor cell operating in the triode or saturation region. It achieves a high linearity range of ± 1 V at a 1.5 V supply voltage. The proposed transconductor is used to realize a new fully-differential Gm-C low-pass filter with a minimum number of transconductors and grounded capacitors. PSpice simulation results for the transconductor circuit and its filter application indicating the linearity range and verifying the analytical results using 0.35 μm technology are also given.

Keywords: CMOS transconductor, Gm-C filters.

I. Introduction

Transconductance elements are useful building blocks in analog signal processing systems, especially in continuous time filters [1]-[15]. Transconductance-C or Gm-C filters have recently received great interest since they are suitable for integration and can operate at high frequencies. Although on-chip active filters consume power, chip area, and limit the overall dynamic range, they enable high integration and bandwidth tuning [1]. Therefore, the design of highly linear and tunable transconductors has become mandatory.

Several realizations for CMOS transconductors have been introduced in the literature [2]-[12]. The realization given in [2] is based on using a differential stage with MOS transistors operating in the saturation region with their sources connected to their substrates. The realizations given in [3] and [4] provide a CMOS transconductor with a balanced output current based on the use of a wide input range differential transconductor. The CMOS transconductor given in [5] is based on the use of a simple MOS differential pair. The use of a four-MOS transistor cell to realize CMOS transconductors was first introduced by Czarnul [6] and used in [7] through [9]. The realization given in [10] is based on the use of MOS transistors operating in the non-saturation region, while the one given in [11] is based on the use of multiple-input floating gate transistors. The use of a cross-coupled quad-cell-based input stage together with an additional linearizing symmetrical differential pair was given in [12].

In this paper, a new CMOS fully-differential transconductor is presented. Fully-differential transconductor structures avoid the use of a current mirror for current subtraction, as in single-ended transconductors, by generating two output currents and effectively performing the subtraction by taking the output current across two nodes instead of at a single node referred to

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Mohamed O. Shaker (email: moh_o_a@hotmail.com) and Ahmed M. Soliman (phone: + 202 5678822, email: asoliman@idsc.net.eg) are with Department of Electronics and Communications, Cairo University, Cairo, Egypt.

Soliman A. Mahmoud (email: amahmoud@frcu.edu) is with Department of Electrical Engineering, Cairo University, Fayoum, Egypt.

ground [13]. The structure of the proposed transconductor depends on a four-MOS transistor cell to obtain a linear transconductor with a wide input operating range.

The basic structure of the fully-differential transconductor and its symbol are shown in Figs. 1(a) and 1(b), in which the voltage-to-current converter (V-I) generates two output currents, I_{o1} and I_{o2}, where output current I_o is linearly proportional to the differential input voltage $(V_1 - V_2)$ such that

$$I_o = I_{o2} - I_{o1} = I_a - I_b = G(V_1 - V_2), \quad (1)$$

where G is the equivalent transconductance.

In section II, the realization of the CMOS fully-differential transconductor is introduced. In section III, the proposed transconductor is used to design a new fully-differential third-order low-pass filter with a minimum number of components and grounded capacitors. Finally, conclusions are stated in section IV. PSpice simulation results for the transconductor circuit indicating the linearity range and confirming the analytical results are also given.

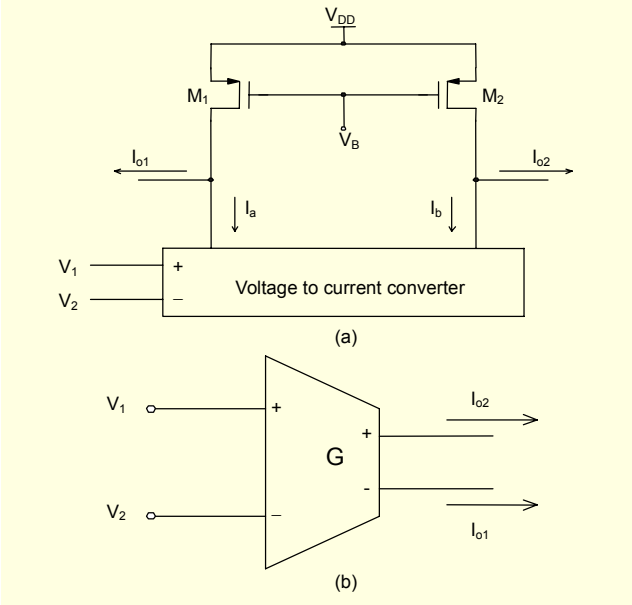

Fig. 1. (a) The basic structure of the fully-differential transconductor and (b) the symbol of the fully-differential transconductor.

II. The CMOS Fully-Differential Transconductor

The structure of the proposed CMOS fully-differential transconductor depends on the four-MOS transistor cell, as shown in Fig. 2. In Fig. 2, the input voltage V_1 is connected to the gates of M_1 and M_4, and the input voltage V_2 is connected to the gates of M_2 and M_3. This four-transistor cell was used to realize fully-integrated CT filters under the condition where four transistors are operating in the triode region and the drain voltages of the four transistors are equal (V_{D1}=V_{D2}). Using the

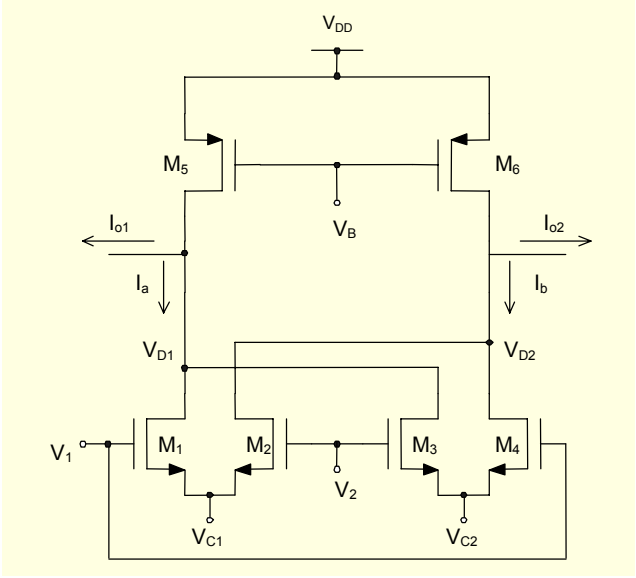

Fig. 2. The CMOS circuit of the four-MOS transistor cell [6].

current in the triode region of an NMOS transistor as a function of the gate (V_G), drain (V_D), source (V_S), and threshold (V_T) voltages given in [14] by

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + \cdots, \quad (2)$$

$$K = \mu_n C_{ox} \cdot \frac{W}{L}, \quad (3)$$

where μ_n is the electron mobility; C_{ox} is the gate oxide capacitance per unit area; W/L is the transistor aspect ratio; V_T is the threshold voltage (assumed equal for all NMOS transistors); and K is the transistor transconductance parameter. Assuming that all body terminals are connected to the proper supply voltages, the differential output current is given by

$$I_o = I_{o2} - I_{o1} = I_a - I_b = K(V_{C2} - V_{C1})(V_1 - V_2), \quad V_1(\text{or } V_2) \geq V_{D1} + V_T, \quad V_1(\text{or } V_2) \geq V_{D2} + V_T. \quad (4)$$

Therefore, a linear relation between the differential output current $I_{o1} - I_{o2}$ and the differential input voltage $(V_1 - V_2)$ can be obtained with V_{C1} and V_{C2} being independent of V_1 and V_2. Therefore, the transconductance G is given by

$$G = K(V_{C2} - V_{C1}), \quad (5)$$

which can be controlled by the differential voltage $V_{C2} - V_{C1}$.

It is interesting to note that by using the square-law equation of the drain current in the saturation region given by I_D=$(K/2)(V_{GS}–V_T)^2$, the same relation between the differential output current $I_{o2} - I_{o1}$ and the differential input voltage $(V_1 - V_2)$ as given in (4) is obtained. Therefore, proper operation for

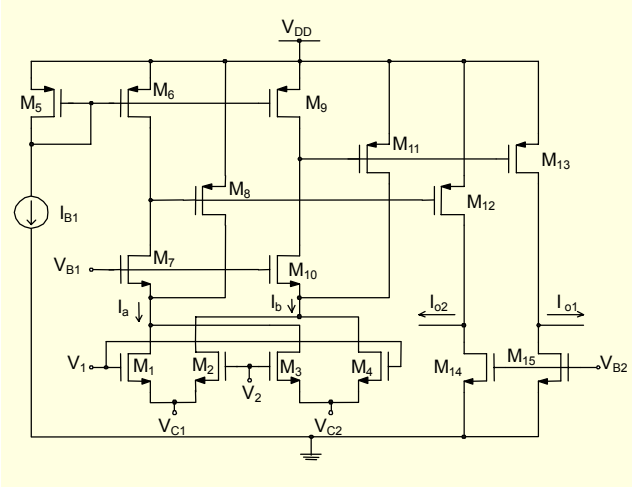

Fig. 3. The CMOS circuit of the proposed fully-differential transconductor.

the input voltages V_1 and V_2 is to make the four transistors 'on' provided that the drain voltages are equal. The proposed CMOS transconductor shown in Fig. 3 is formed using M_1 to M_4 as the basic MOS transistors; M_5, M_6, and M_9 as current sources; and M_7 and M_{10} as source followers, where M_{12} and M_{13} sense the current in M_8 and M_{11}, respectively, while M_{14} and M_{15} are used as constant current sources. The loop formed by M_7 and M_8 ensures that the voltage at the source of M_7 is constant and can be obtained as

$$I_7 = I_{B1} = \frac{K_7}{2}[V_{B1} - V_{S7} - V_T]^2, \quad (6)$$

$$V_{S7} = V_{B1} - [V_T + \sqrt{\frac{2I_{B1}}{K_7}}]. \quad (7)$$

The role of transistor M_8 is to form a negative feedback action, which provides the necessary currents needed by transistors M_1 and M_3 without changing the voltage so as to satisfy (7).

Similarly, the loop formed by M_{10} and M_{11} operates in the same manner, hence

$$V_{S10} = V_{B1} - [V_T + \sqrt{\frac{2I_{B1}}{K_{10}}}]. \quad (8)$$

If M_7 and M_{10} are matched, then from (7) and (8),

$$V_{S7} = V_{S10} = V_{B1} - [V_T + \sqrt{\frac{2I_{B1}}{K_7}}]. \quad (9)$$

And the input voltage range will be increased to

$$V_1(\text{or } V_2) \geq V_{C1} + V_T, \; V_1(\text{or } V_2) \geq V_{C2} + V_T. \quad (10)$$

The circuit shown in Fig. 3 can be extended to realize a multiple output transconductor by repeating the output stage, which consists of transistors M_{12} through M_{15} as shown in Fig. 4. Performances of both the four-MOS transistor cell and the proposed fully-differential transconductor are simulated using PSpice. The transistor aspect ratios of the proposed

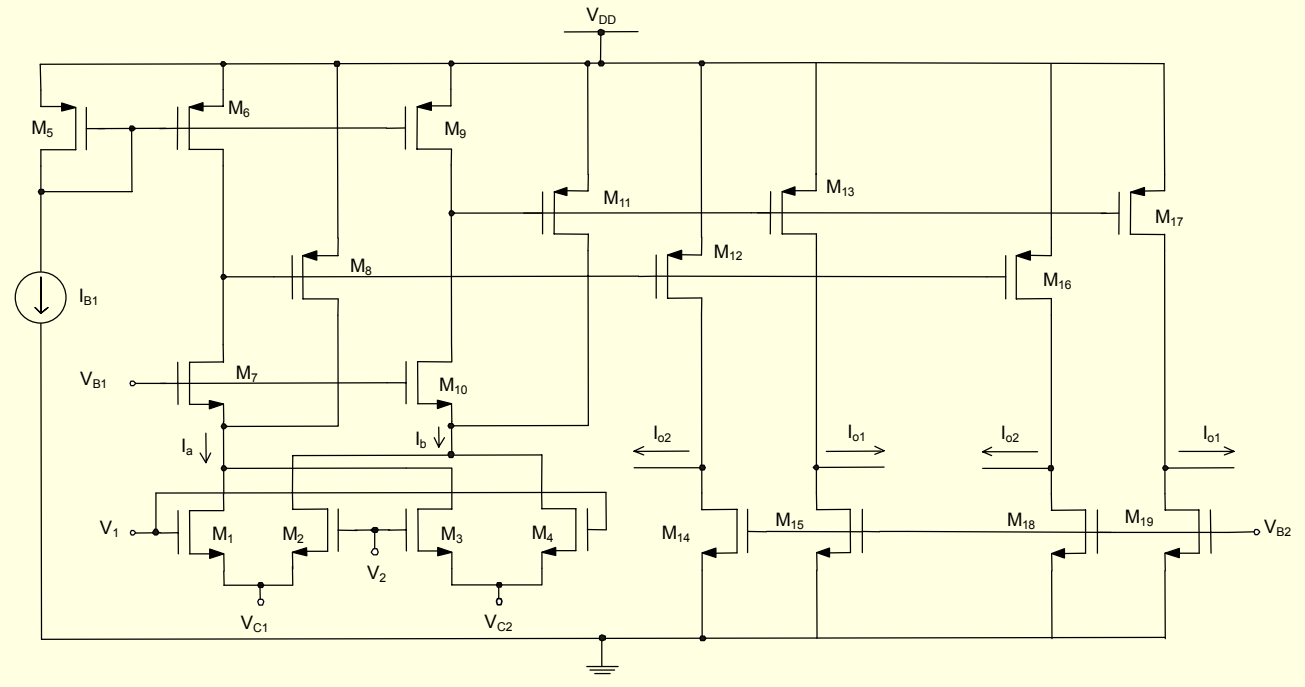

Fig. 4. The CMOS circuit of the proposed multiple output transconductor.

transconductor are give in Table 1. The supply voltage used is given by V_{DD} = 1.5 V, I_{B1} is set to 120 μA, and the control voltages used are given by V_{C1} = -1.5 V, V_{C2} = -1.2 V to keep the basic transistors M_1 through M_4 on and to satisfy (10). Figure 5 shows the differential output current for the proposed transconductor versus ($V_1 - V_2$), which is scanned from –1 V to 1 V, compared with that of the four-MOS transistor cell. It is seen

Table 1. Transistor aspect ratios of the proposed transconductor.

Transistors	Aspect ratio (W/L)
M_5, M_6, M_9	64/2
M_1, M_2, M_3, M_4	8/2
M_8, M_{11}, M_{12}, M_{13}	40/2
M_7, M_{10}	96/2
M_{14}, M_{15}	10/2

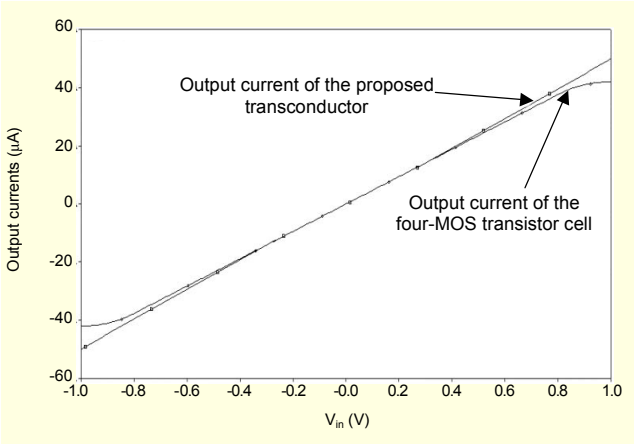

Fig. 5. The DC output current of the proposed fully-differential transconductor.

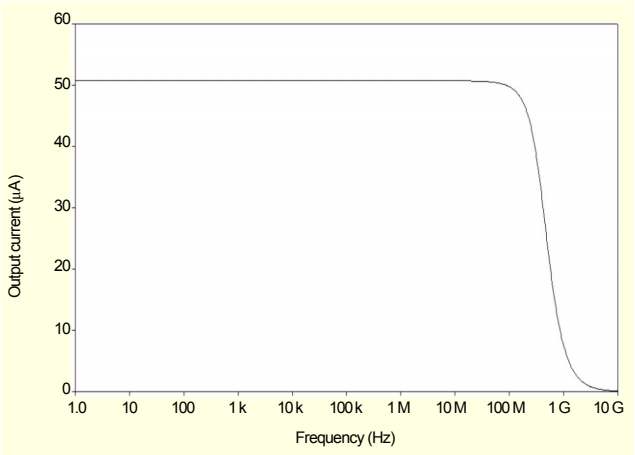

Fig. 6. The magnitude frequency response of the proposed fully-differential transconductor.

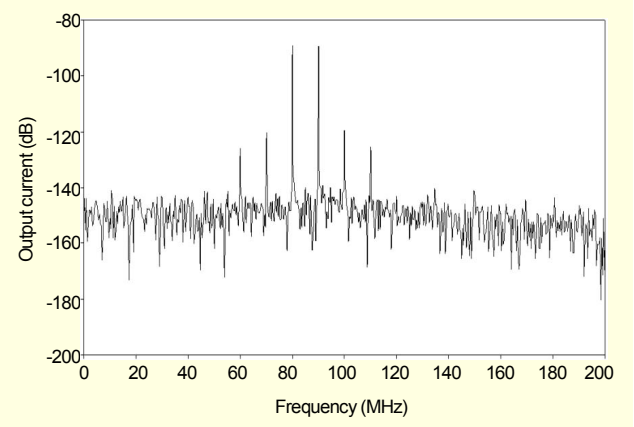

Fig. 7. The simulated IM3 frequency spectrum of the proposed fully-differential transconductor output current at input frequencies of 80 and 90 MHz and at input voltages of 1 V_{p-p}.

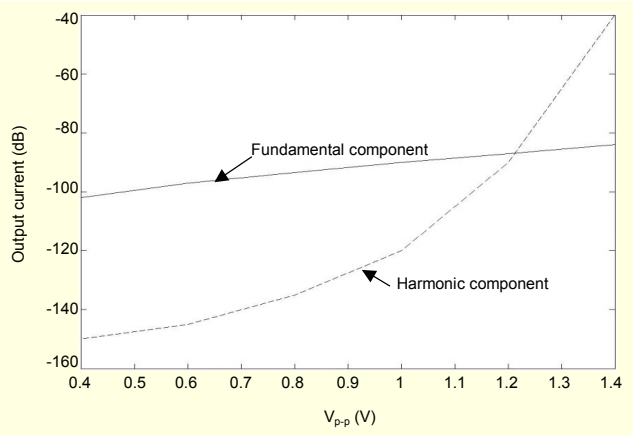

Fig. 8. The IP3 plot of the proposed fully-differential transconductor output current at input frequencies of 80 and 90 MHz.

that the linearity range becomes wide and that the transconductance of the proposed transconductor seems constant over a wide range. Simulation results showed that the 3 dB frequency of the proposed transconductor when terminated by 1 KΩ is 300 MHz as shown in Fig. 6. Figure 7 shows the third-order intermodulation (IM3) of the differential output current when 1 V_{p-p} sinusoidal voltage signals of 80 MHz and 90 MHz are applied at the input. The IM3 is about 30 dB. The input of the third intercept point (IIP3) is equal to 1.2 V_{p-p}, which can be obtained directly from the third intercept point (IP3) plot shown in Fig. 8.

III. The Proposed Fully-Differential Filter

Any active filter implementation requires basic functions such as integration, lossy integration, and addition [15]. The addition or subtraction in the filters based on differential transconductors is achieved by simply connecting the output of the transconductors that deliver the signal to be summed. In

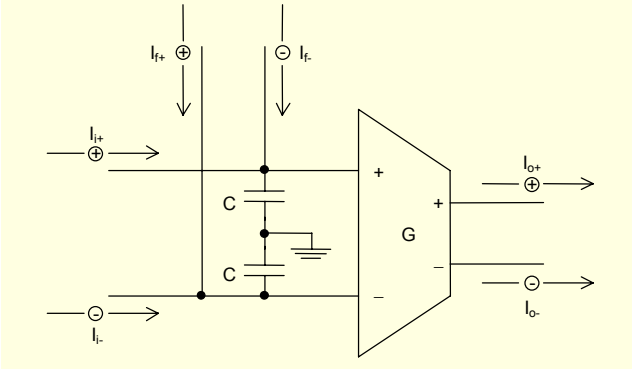

Fig. 9. The symbol of the differential current integrator.

this section, the application of the proposed transconductor to realize a fully-differential low-pass third-order filter is given.

A. Integrator

The basic building block in the construction of Gm-C filters is the integrator. The symbol of the differential current integrator is shown in Fig. 9, in which the differential output current can be obtained as

$$I_o = \frac{G}{sC}(I_i - I_f), \tag{11}$$

where $I_o = I_{o+} - I_{o-}$ is the differential output current, $I_i = I_{i+} - I_{i-}$ is the differential input current, and $I_f = I_{f+} - I_{f-}$ is the differential feedback current.

B. New Fully-Differential Low-Pass Third-Order Filter

An example of the use of the proposed differential transconductor in the realization of an active filter is shown in Fig. 10. The filter has low-pass output in a differential form. The circuit includes three transconductors and six grounded capacitors, which makes the filter suitable for very-large-scale-integration implementation. The transfer function of the low-pass output is given by

$$\frac{I_o}{I_i} = \frac{1}{\tau_1\tau_2\tau_3 s^3 + (\tau_2\tau_3 + \tau_1\tau_3)s^2 + 2\tau_3 s + 1}, \tag{12}$$

where the time constant $\tau_j = C_j/G_j$.

Figure 11 shows the PSpice simulation results of the Gm-C filter using the proposed transconductor with $G_1 = G_2 = G_3 = 50$ μA/V and $C_1 = C_2 = C_3 = 0.4$ pF to obtain a maximally flat magnitude low-pass response designed for a DC gain of 1 and $f_o = 20$ MHz. It is clear that the ideal and actual responses are almost identical at low frequencies, but there is a difference at high frequencies due to parasitic effects, which can be reduced by using compensation methods. Figure 12 shows the IM3 of

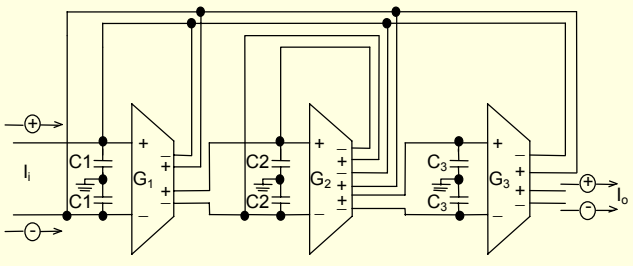

Fig. 10. The third-order low-pass Gm-C filter.

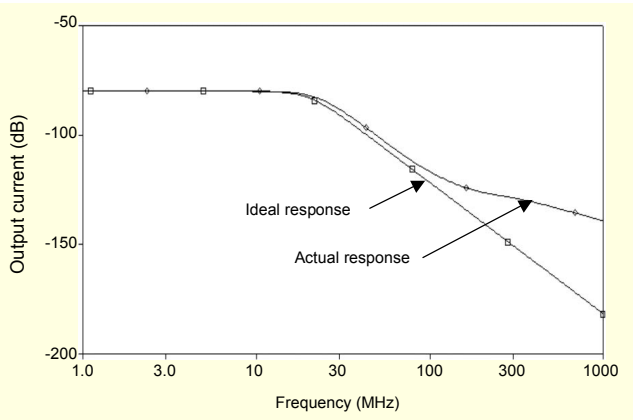

Fig. 11. The magnitude frequency response of the third-order low-pass filter.

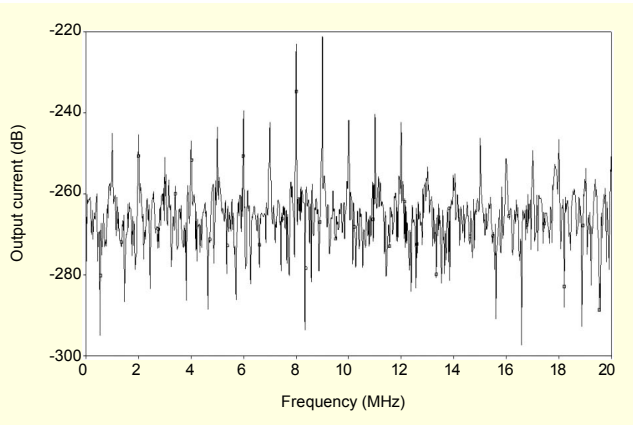

Fig. 12. The simulated IM3 frequency spectrum of the proposed Gm-C output current at input frequencies of 8 and 9 MHz.

the differential output current when sinusoidal current signals of 8 and 9 MHz are applied at the input. The IM3 is about 20 dB due to the use of a wide linear transconductor.

IV. Conclusions

In this paper, a tunable transconductor based on the four-MOS transistor cell, which can operate in the linear or saturation region, has been presented. A third-order maximally flat low-pass filter with a minimum number of blocks, which is

based on lossless/lossy integrators, has been introduced. The proposed blocks and their applications have been confirmed using PSpice simulation.

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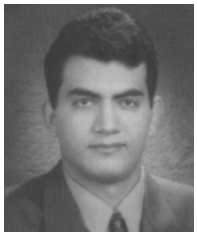
Mohamed O. Shaker was born in Fayoum, Egypt, in 1979. He received the BSc degree with honors in electrical engineering from Cairo University, Fayoum Campus, Fayoum, Egypt, in 2001, and the MSc degree in electronics and communications engineering from Cairo University, Cairo, Egypt, in 2005. He is currently a Teaching Assistant in the Radiation Engineering Department, Egyptian Atomic Energy Authority. His research interests include analog CMOS-integrated circuit design and signal processing, circuit theory, and fully integrated analog filters.



Soliman A. Mahmoud was born in Cairo, Egypt, in 1971. He received the BSc degree with honors in 1994, the MSc degree in 1996, and the PhD degree in 1999, all from the Electronics and Communications Department, Cairo University, Egypt. He is currently an Associate Professor at the Electrical Engineering Department, Cairo University, Fayoum Campus. He has published more than 50 papers. His research and teaching interests are in circuit theory, fully-integrated analog filters, high-frequency transconductance amplifiers, low-voltage analog CMOS circuit design, current-mode analog signal processing, and mixed analog/digital programmable analog blocks.

Ahmed M. Soliman was born in Cairo Egypt, on November 22, 1943. He received the BSc degree with honors from Cairo University, Cairo, Egypt, in 1964, and the MS and PhD degrees from the University of Pittsburgh, PA, USA, in 1967 and 1970, all in electrical engineering. He is currently a Professor in the Electronics and Communications Engineering Department, Cairo University, Egypt. From September 1997 to September 2003, he served as a Professor and Chairman of the Electronics and Communications Engineering Department, Cairo University, Egypt. From 1985 to 1987, he served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987 to 1991 he was the Associate Dean of Engineering at the same university. He has held visiting academic appointments at San Francisco State University, Florida Atlantic University, and the American University in Cairo. He was a Visiting Scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987). In 1977, He was decorated with the First Class Science Medal from the President of Egypt for his services to the field of Engineering and Engineering Education. He is a Member of the Editorial Board of the IEE Proceedings Circuits, Devices and Systems and a Member of the Editorial Board of Analog Integrated Circuits and Signal Processing. He also served as Associate Editor of the IEEE Transactions on Circuits and Systems I (Analog Circuits and Filters) from December 2001 to December 2003 and has been Associate Editor of the Journal of Circuits, Systems and Signal Processing since January 2004.