A New Low-Voltage CMOS Rail-to-Rail Balanced Output Current Conveyor Realization

Ahmed H. Madian
Egyptian Atomic Energy Authority
Cairo, Egypt.
ah_madian@hotmail.com

Soliman A. Mahmoud,
Electrical Engineering Dept.
Cairo University, Fayoum branch.
Fayoum, Egypt.

Ahmed M. Soliman
Electronics and communications
Dept. Cairo University.
Giza, Egypt

***Abstract*— In this paper, a new CMOS low-voltage second generation balanced output current conveyor (BOCCII) introduced. The BOCCII has provided an n-channel differential pairs voltage follower stage instead of complementary differential pairs to provide a rail-to-rail input/output operation. A high driving current capability ensured by using a class AB topology output stage. For the proposed BOCCII, the static power consumption is 5.22mW, the open circuit input-referred noise voltage is 5μV/$\sqrt{Hz}$, THD is -53dB, and IM3 is -42.7dB. PSpice simulations for the new BOCCII are given using 0.35μm CMOS technology and ±1V supply voltage to verify the analytical results.**

I. INTRODUCTION

The second-generation current conveyor (CCII) proposed by Sedra and Smith in [1] has proved to be a functionally flexible and versatile block. The CCII modeled as a three terminal block derived by interconnecting a voltage and current followers. An ideal CCII has infinite impedance at Y and Z terminals and zero impedance at X terminal. The voltage at X terminal follows the voltage at Y terminal and the current at Z terminal follows that at X terminal. The Z terminal current direction relative to that at X terminal defines whether CCII is positive or negative. The balanced output CCII (BOCCII), shown in fig. 1, provides both the negative and positive Z terminals output. The input/output relation could be described with equation (1),

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

Several CCII structures have realized [1-9]. These structures aimed to improve the voltage and the current transfer accuracy [2], increasing the output current capabilities [6-9], while reducing the offset using a several compensation techniques [3]. In addition, a fully differential behavior realization has presented [6]. To extend the region of operation up to rail-to-rail, the input stage is typically made-up of two parallel connected complementary (i.e. n-channel and p-channel) differential pairs [9]. Unfortunately, it includes a class A output stage which limits the maximum output current achievable. Although in the same paper [9] a small arrangement providing class AB behavior suggested. However, with this approach the small signal and large-signal behaviors suffer from large deviations when the input voltage sweeps entire voltage range and increases the supply requirements to a value higher than ±1.5V. Reference [8] has provided a solution to overcome this drawback. The solution offers a close rail-to-rail input and output ranges, as well as a high driving current capability. Using the same input stage is typically made-up of two parallel connected complementary. There is a draw back that once transistors have been properly sized to operate under a certain supply voltage, this voltage cannot be modified substantially.

In this paper, a new CMOS low-voltage rail-to-rail BOCCII circuit is proposed. The new circuit uses two n-channel differential pairs voltage as a voltage follower stage instead of complementary differential pairs to provide a rail-to-rail input/output operation. The current follower stage implemented using class AB topology to offer a high-drive current capability with a rail to rail swing capability. The symbol diagram for Balanced output CCII shown in fig. 1. This paper is organized as follows. The basic building block of the proposed BOCCII described in Section 2. In Section 3, PSpice simulations have been carried out to verify the performance of the proposed BOCCII. Conclusion has been reported in Section 4.

Figure 1. The block diagram for BOCCII

0-7803-9197-7/05/$20.00 © 2005 IEEE.

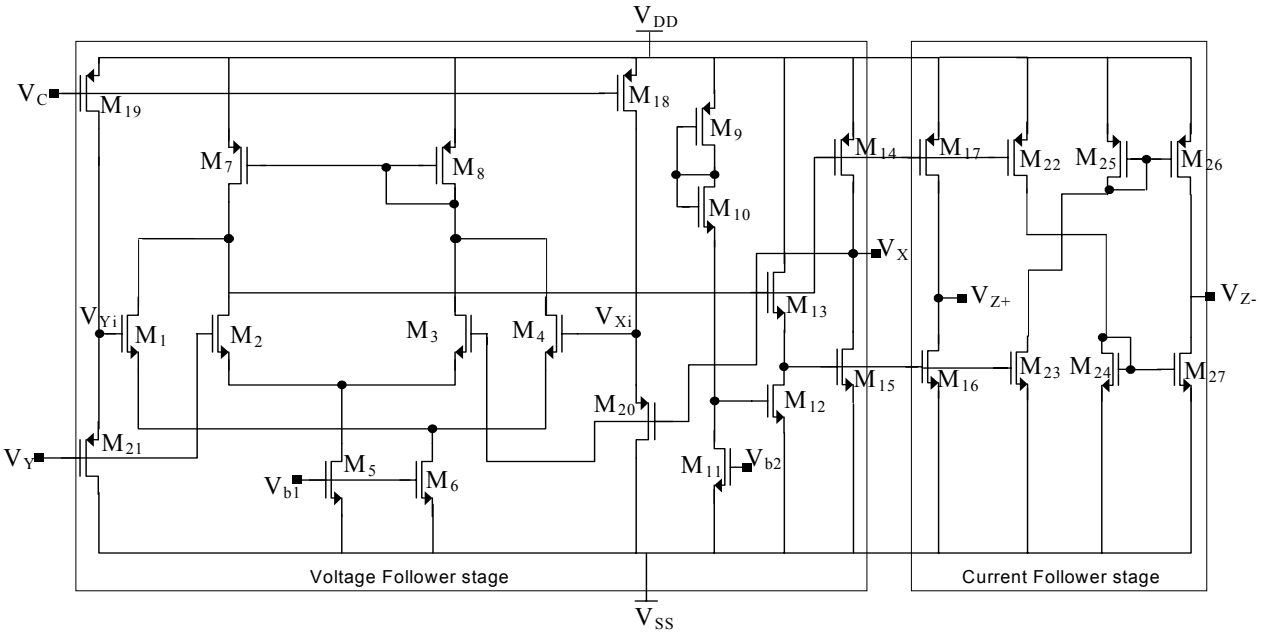

Figure 2. The proposed CMOS low-voltage class AB BOCCII

II. THE PROPOSED BOCCII CIRCUIT DESCRIPTION

Fig. 2 shows the CMOS realization of the proposed BOCCII circuit. The circuit could be divided into two stages: (a) voltage follower stage and (b) current follower stage.

A. Voltage follower stage

The voltage follower implemented using two n-channel differential pairs M_1-M_4 and M_2-M_3, biased with the same current. Two floating voltage sources, implemented by two identical source followers, M_{18}-M_{21}, and M_{19}-M_{20}, connected in front of the Y, X terminals of one of the differential pairs M_1-M_4. These followers provide a positive voltage shift to the Y and X terminals. Transistors M_{18}-M_{20} and M_{19}-M_{21} are matched and have the same feature size.

$$V_{Yi} = V_Y + (V_{DD} - V_C) \tag{2}$$

To ensure a rail-to rail operation, the voltage shift must keep the corresponding input pair active (M_1-M_4) when the other differential pair is inactive (M_2-M_3). The current mirror formed with transistors (M_7-M_8) forces the currents in transistors M_1, M_2 equal to the currents in transistors M_3, M_4 and hence:

$$V_X = V_Y \tag{3}$$

The X terminal voltage V_X follows the Y terminal voltage V_Y.

To provide low impedance at the X terminal, a suitable buffer should be used. Traditional source follower is not suitable since it will not provide a rail to rail swing capability. In the proposed circuit, a class AB buffer is used to ensure rail to rail swing capability. Transistors M_{14} and M_{15} form the push-pull output stage at the X terminal. Transistors M_{12} and M_{13} are level shifting to provide the proper biasing for M_{15}. Both transistors M_{14} and M_{15} must be on when no current is withdrawn from the X terminal. This current, standby current, should be small and controllable. This achieved by using a suitable gate voltage M_{11} that sets the voltage level shift between the gates of M_{14} and M_{15}. Assuming all transistors to be working in saturation region, it is clear that:

$$V_{SG14} + V_{GS13} + V_{GS15} = V_{DD} - V_{SS} \tag{4}$$

And,

$$V_{SG9} + V_{GS10} + V_{GS12} = V_{DD} - V_{SS} \tag{5}$$

B. Current follower stage

The current follower stage implemented using transistors M_{16} and M_{17} to convey the X terminal current to the Z_+ terminal.

$$I_{Z+} = I_X \tag{6}$$

By using extra current mirrors, as shown in fig. 2, transistors M_{22}-M_{27} the negative output current Z_- could be realized.

$$I_{Z-} = -I_X \tag{7}$$

The small signal output resistance at the Z terminal could be given by:

$$r_z = r_{o16} \,//\, r_{o17} \tag{8}$$

By inspection of the whole circuit, the minimum supply voltage requirement by the input differential stage is V_T+3V_{DSsat}.

III. SIMULATION RESULTS

The circuit, shown in fig. 2, has been simulated using PSpice with 0.35µm CMOS technology from MOSIS. The power supply voltages V_{DD} and V_{SS} are balanced (1V and -1V) respectively, Vc = 0.65V, the output current was sensed using 1kohm output resistance at the X, Z_+ and Z_- terminals. Table I gives the proposed BOCCII transistors aspect ratios. Fig. 3 presents the output voltages V_X, V_{Z+} and V_{Z-} versus V_Y, a rail-to-rail operation has been obtained. The X, Z_+ and Z_- terminals are terminated with 5kΩ output resistances and V_Y varied from -1V to 1V. Fig. 4 shows the X terminal offset voltage variation versus I_X while the Y, Z_+ and Z_- terminals grounded, and I_x varied from -1.5mA to 1.5mA. The X terminal output resistance has been obtained as 0.522Ω. The stability of the new BOCCII is verified by simulating the transient response for a ±0.5V input step of 0.1µs rise time and frequency 0.25 MHz; the corresponding result is shown in fig. 5. The 0.1% settling time is lower than 1µs. The phase shift between the Z_+ and Z_- output voltages is 180^0. The open-circuit frequency response between the X and Y terminals is shown in fig. 6, where V_Y is the AC-varying signal with 1V magnitude, the X and Z terminals terminated with resistances 1kΩ. The open circuit bandwidth is around 1.5MHz. Fig. 7 indicates the short circuit frequency response between the X terminals and the Z_+ and Z_- terminals. The short circuit bandwidth is around 1.1MHz. Fig. 8 gives the IM3 spectral density of the new BOCCII for two input signals with frequencies 0.5 kHz, 1 kHz and 0.5Vpp magnitude. From the transient simulations the IM3 could be obtained as -42.7dB. The input-referred noise voltage spectral densities for the BOCCII when terminated by 1kΩ is equal to $5\mu V/\sqrt{Hz}$. The maximum current driving capability of the proposed BOCCII is greater than 850µA. Table II summarizes the simulation results of the proposed BOCCII.

TABLE I. THE PPROPOSED BOCCII TRANSISTOR ASPECT RATIOS

Transistors	W (µm)	L (µm)
M_1-M_4,	2.8	0.7
M_5,M_6	4.2	1.4
M_7, M_8	28.7	7
M_{10}, M_{11}	0.7	0.7
M_9, M_{21},M_{20}, M_{18},M_{19}	1.4	0.7
M_{15}, M_{16}, M_{23}, M_{24}, M_{27}	94.85	1.4
M_{14}, M_{17}, M_{22}, M_{25}, M_{26}	250.25	1.4
M_{12}, M_{13}	4.2	1.4

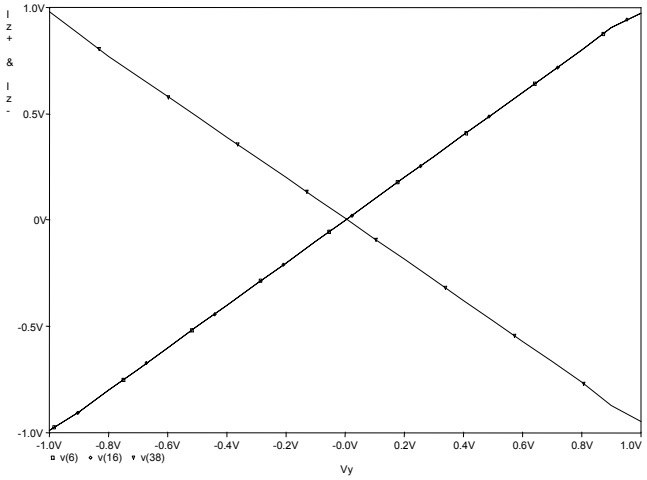

Figure 3. The output voltages V_X, V_{Z+} and V_{Z-} versus V_Y varying from -1v to 1v

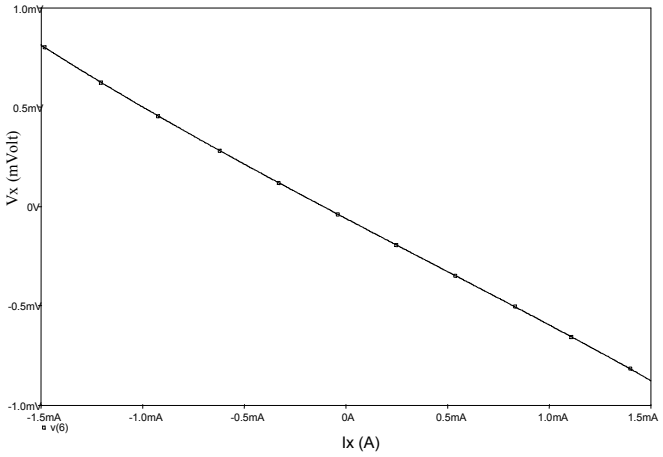

Figure 4. The X terminal offset voltage while Z & Y terminals grounded

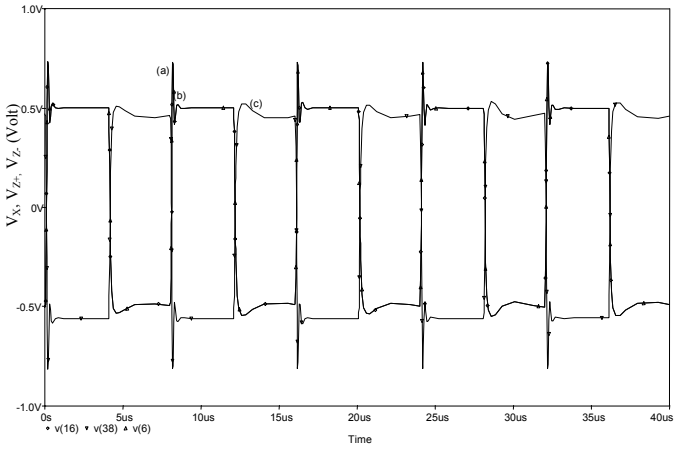

Figure 5. The proposed BOCCII transient response (a) the X, (b) the Z+ and (c) the Z- ,output voltages

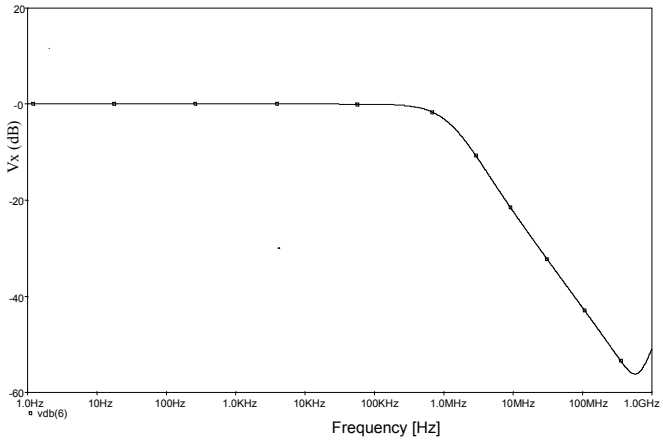

Figure 6. The X terminal open circuit frequency response

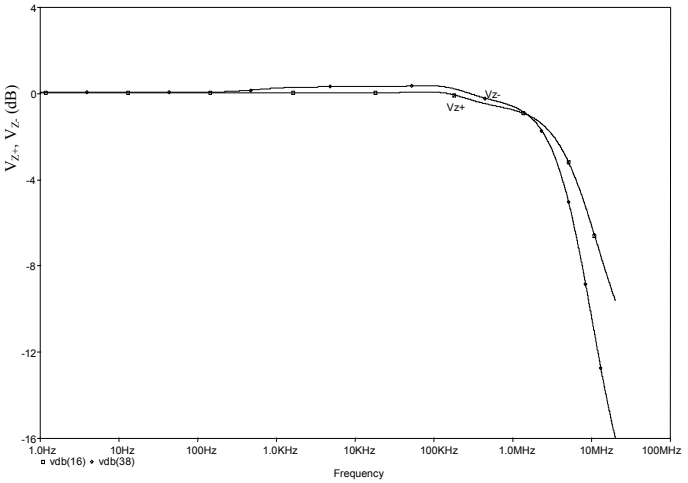

Figure 7. The short circuit frequency response V_{Z+} and V_{Z-}

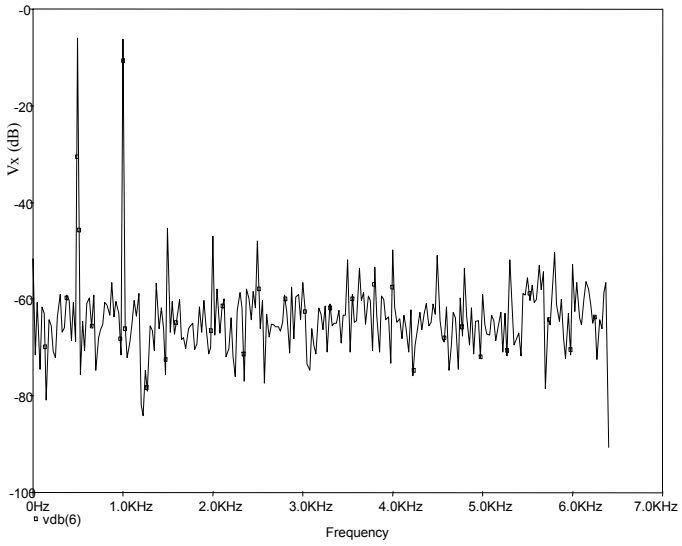

Figure 8. The two tone IM3 spectral density of the proposed BOCCII

TABLE II. SUMMARY OF THE SIMULATED RESULTS FOR THE PROPOSED BOCCII

CMOS Technology	0.35µm
Power supply (V_{DD}, V_{SS})	(1V,-1V)
The 0.1% settling time	<1µs
Total Power dissipation	5.2 mW
The open circuit X terminal THD @ V_Y=0.5*sin (2ΠIf) V, f =1kHz.	-53.18dB
Input Voltage Dynamic range (Ix= 0A)	-1V to 1V
The X terminal offset voltage while Y and Z are grounded	< 0.9 mV
Current driving capability (R_X=R_Z = 500Ω)	±1.5mA
Voltage transfer error	-0.02dB
R_X	0.522 Ω
Current transfer error	-0.024dB
The X terminal open circuit B.W.	1.5 MHz
The Z terminal short circuit B.W.	1.1 MHz
The two tone IM3 @ $f_{1,2}$ = 0.5kHz, 1kHz, 0.5V_{pp}. IM3 = $\frac{a_{@\,2\omega_1+\omega_2}}{a_{@\,\omega 1}}$	-42.7 dB

IV. CONCLUSION

In this paper, a new CMOS low voltage BOCCII has presented. The proposed circuit performance has confirmed by using PSpice simulations with 0.35µm technology, and supply voltage ±1V. It shows a good overall performance. The simulations included the power consumption, the frequency bandwidth, input referred noise, IM3 and THD, as given in table II.

REFERENCES

[1] C. Smith and S. Sedra, "The current conveyor-a new circuit building block," IEEE Proc., vol.56, pp. 1368-1269, 1968.

[2] H. O. Elwan and A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications," IEE Proc.-circuits devices syst., vol.144, pp. 195-200, 1997.

[3] I. A. Awad and A. M. Soliman, "Inverting second generation current conveyor: the missing building blocks, CMOS realizations and applications," Int. J. Electronics, vol. 86, pp. 413-432, 1999.

[4] A. M. Soliman, "Generation of current conveyor-based all-pass filters from op-amp based circutis," IEEE trans. on circuits and syst. II, analog and digital signal processing, vol. 44, no.4, April 1997.

[5] S. A. Mahmoud and A. M. Soliman, "A new CMOS programmable balanced output transconductor and applications to a mixed mode universal filters suitable for VLSI," analog integrated circuits and signal processing, vol. 19, pp. 241-254, 1999.

[6] S. A. Mahmoud and I. A. Awad, "Fully differential CMOS current feedback operational amplifier," analog integrated circuits and signal processing, vol. 43, pp. 61-69, 2005.

[7] S. A. Mahmoud and A. M. Soliman, "New MOS-C biquad filter using the current feedback operational amplifier," IEEE Trans. Circuits Syst.I, Fundam. Theory Appl., vol. 46, no. 12, pp. 1510–1512, 1999.

[8] R. Mita, G. Palumbo and S. Pennisi, "1.5-V CMOS CCII+ with high current-driving capability," IEEE trans. on circuits and Syst. II, analog and digital signal processing, vol. 50, no. 4, 2003.

[9] H. O. Elwan and A. M. Soliman, "Low-voltage low-power CMOS current conveyors," IEEE transaction on circuits and syst. I, fundamental theory and applications, vol. 44, no. 9, 1997.