Low-Voltage CMOS Current Feedback Operational Amplifier and Its Application

Soliman A. Mahmoud, Ahmed H. Madian, and Ahmed M. Soliman

A novel low-voltage CMOS current feedback operational amplifier (CFOA) is presented. This realization nearly allows rail-to-rail input/output operations. Also, it provides high driving current capabilities. The CFOA operates at supply voltages of ±0.75 V with a total standby current of 304 µA. The circuit exhibits a bandwidth better than 120 MHz and a current drive capability of ±1 mA. An application of the CFOA to realize a new all-pass filter is given. PSpice simulation results using 0.25 µm CMOS technology parameters for the proposed CFOA and its application are given.

Keywords: Current feedback op-amp, low-voltage, variable gain amplifier, all-pass filter.

I. Introduction

In recent years, great interest has been devoted to the analysis and design of current feedback op-amp and current-conveyor integrated circuits [1]-[14], mainly because these circuits exhibit better performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers (VOA). The current feedback operational amplifier (CFOA) close-loop bandwidth is independent of its close-loop gain (provided that the feedback resistance is kept constant and much higher than the CFOA inverting input resistance) [7] unlike VOA-based circuits, which are limited by a constant gain-bandwidth product. The CFOA, shown in symbolic form in Fig. 1(a), is a four-port network which has a describing matrix of the following form:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix}. \quad (1)$$

Originally, CFOAs were implemented using only bipolar process technology. This technology is intrinsically well suited to process signals in the form of currents giving the high bipolar junction transistor (BJT) transconductance. More recently, several CMOS realizations for the CFOA have been reported in the literature [4]-[7], [9]-[14]. The CFOA has always been seen as an extension of the second generation current conveyor (CCII); therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [2]. The obtained bandwidth was always a degraded version of the CCII+ bandwidth. Several CMOS CFOA implementations have been presented to provide offset

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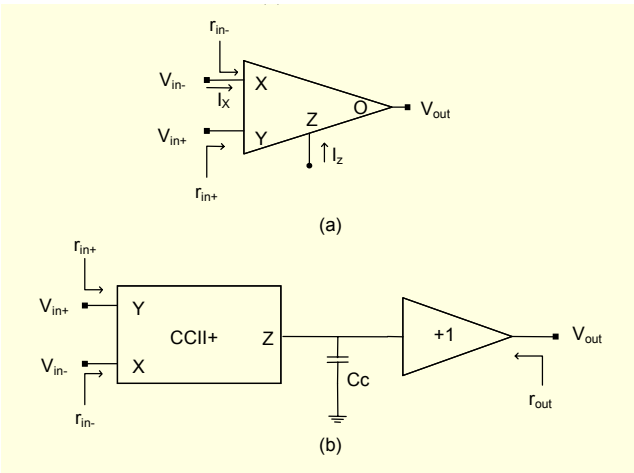

Fig. 1. (a) Current feedback op-amp symbol and (b) CFOA block diagram [2].

compensation [4], high current drive capability [6], [7], and suitability for high frequency applications compensation [5]. The low-power/low-voltage issue, which is increasingly important in very large scale integrated (VLSI) circuits, was partially addressed in [12].

In this paper, a novel CMOS current-feedback operational amplifier is presented. The CFOA is capable of operating under a minimum supply voltage ($|V_{Tp}|+V_{Tn}+V_{DS,sat}$) and with reduced power dissipation. The new circuit includes a class AB output stage exhibiting high current drive capability and good power conversion efficiency. A rail-to-rail input and output voltage operation is also nearly achieved.

This paper is organized as follows. In section II, the circuit description and CMOS realization of the proposed CFOA are illustrated. In section III, PSpice simulations of the proposed CFOA using CMOS 0.25 μm technology are also given. In section IV, an application of the CFOA to realize a new all-pass filter structure is given. In section V, conclusions are drawn.

II. Proposed CMOS Current Feedback Op-Amp

As stated in the introduction, the CFOA could be realized by the CCII which is cascaded with a voltage follower [2], as shown in Fig. 1(b). The CMOS realization of the proposed CFOA, which offers both low-voltage and high drive capability will be described.

The CMOS realization of the proposed CFOA shown in Fig. 2 consists of two matched parallel connected n-differential pairs, (M_1, M_2) and (M_3, M_4); two matched biasing current source transistors, (M_5, M_6); a cascoded current mirror formed of matched transistors, (M_7, M_8, M_9); and two pairs of matched source follower transistors, (M_{10}, M_{11}) and (M_{12}, M_{13}). Transistors M_5 and M_6 carry equal bias currents (I_B), while transistors (M_{10}, M_{11}) and (M_{12}, M_{13}) produce a positive voltage shift for the input voltage applied on transistors M_{11} and M_{13}. All transistors are operating in the saturation region; the control voltage V_C applied to transistor gates M_{10} and M_{12} controls the shifting value as

$$V_{Yi} = V_Y + (V_{DD} - V_C), \tag{2}$$

$$V_{Xi} = V_X + (V_{DD} - V_C), \tag{3}$$

where V_{Yi} and V_{Xi} are the output voltages from the source followers, V_Y is the high input impedance voltage, and V_X is the low input impedance terminal.

The circuit regions of operation can be explained as follows: V_Y and V_X voltages are closed to the negative supply voltage V_{SS} ($V_{SS} \le V_Y$, $V_X < 2V_{Tn} + V_{SS}$), so the current source transistor M_5 and, hence, the differential pair M_3 and M_4 are cut-off. Therefore, the small and large signal behaviour of the whole circuit results only from the contribution of the differential pair M_1 and M_2, biased with current source transistor M_6. In the middle range ($2V_{Tn} + V_{SS} \le V_Y$, $V_X < V_C + 2V_{Tn} - 2V_{DD}$), both input pairs (M_1, M_2) and (M_3, M_4) are active and the small and large signal behaviour of the whole circuit results from the contribution of both differential pairs. Finally, when V_Y, V_X are very close to the positive supply voltage V_{DD} ($V_C + 2V_{Tn} - 2V_{DD} \le V_Y$, $V_X \le V_{DD}$), the current sources of the shifters M_{10} and M_{12} are cut-off. Therefore, the small and large signal behaviour of the whole circuit contribution results only from the differential pair M_3 and M_4, biased with current source transistor M_5. This ensures a rail-to-rail operation.

It is apparent that this structure does not provide a constant transconductance over the variations of the input voltages V_Y and V_X. A feed forward section could be added to guarantee a constant transconductance over the variations of the input voltages V_Y and V_X; however, this is not a real drawback so long as the loop gain is sufficiently high. Indeed, variations of the open-loop parameter were greatly reduced by feedback action.

The structure of the CFOA input stage (voltage follower) requires the X terminal to have low input impedance, so a suitable buffer circuit should be used to fulfill this condition and to provide a rail-to-rail swing capability. Transistors (M_{14}-M_{20}) fulfill the required buffering action with a rail-to-rail swing capability, as shown in Fig. 2.

Transistors M_{14} and M_{15} form the push-pull output stage at the X terminal. Transistors M_{16} and M_{17} are level-shifting transistors, providing proper biasing for transistor M_{15}. This push-pull action of transistors M_{14} and M_{15} reduces the power dissipation. To prevent crossover distortion, both transistors M_{14} and M_{15} must be ON when no current is withdrawn from

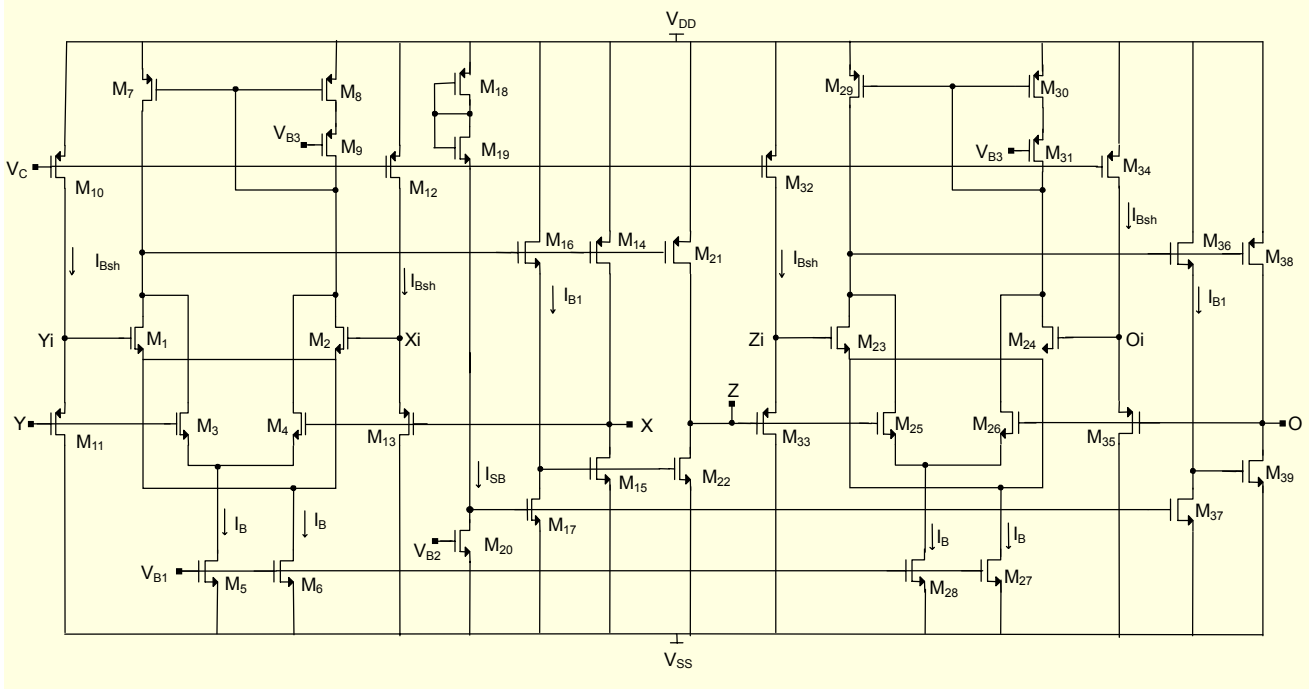

Fig. 2. CMOS realization of the proposed CFOA.

the X terminal (standby mode), this current should be small and controllable. This is achieved by using a suitable gate voltage of M_{20}, which sets the voltage level shift between the gates of M_{14} and M_{15}. The standby power consumption of the overall circuit for dual power supply is given by

$$P_{SB} = 2V_{DD}(4I_{SB} + 4I_B + 4I_{Bsh} + 2I_{B1}). \quad (4)$$

The last term in the above equation is the current passing through the level shift transistors (M_{16}, M_{17}). This current can be kept small by choosing a small aspect ratio for transistors (M_{16}, M_{17}). The class AB output stage enables the circuit to derive the heavy resistive and capacitive load with low standby power dissipation and no slewing. It is worth mentioning that smaller miller compensation capacitors can be connected between the gate and drain of transistors M_{14} and M_{21} to ensure good transient response under all loads.

Transistors M_7 and M_8 force the current in transistors M_1 and M_3 to be equal to the current in transistors M_2 and M_4; therefore,

$$I_{M1} + I_{M3} = I_{M2} + I_{M4}. \quad (5)$$

From the above equation, the matched differential pair transistors carry equal currents; therefore,

$$V_X = V_Y. \quad (6)$$

The current follower stage, as shown in Fig. 2, is made up of transistors (M_{21}, M_{22}). It conveys the X terminal current into the Z terminal current; therefore,

$$I_Z = I_X. \quad (7)$$

Finally, a suitable buffer must be available between the Z and O terminals. It is similar to the buffer between the Y and X terminals and consists of transistors M_{23} to M_{39}; therefore,

$$V_O = V_Z. \quad (8)$$

It is worth mentioning that, the proposed CFOA input stage is a dual circuit. This means that when the input stage which is formed of transistors M_1 to M_6 changes to PMOS, the current source formed from transistors M_7 to M_9 and the biasing circuits M_{10} to M_{12} will be NMOS and vice versa.

For small-signal analysis, when both differential stages are properly working, the open-loop gain T(s) is given by

$$T(s) = \left(\left(\frac{g_{m11}\times(r_{ds11}//r_{ds10})}{1+g_{m11}\times(r_{ds11}//r_{ds10})}\right)\times g_{m1(or\,m2)} + g_{m3(or\,m4)}\right) \times (r_{ds7}//r_{ds1}//r_{ds3})\times g_{m14}\times(r_{ds14}//r_{ds15}). \quad (9)$$

In the above equations, g_{mi} and r_{dsi} are the transconductance and the drain to source resistance of the *i*-th transistor where *i* is the transistor number. As a result for the feedback, as shown in Fig. 2, the voltage gain between the terminals Y and X becomes

$$Av(s) = \frac{V_X(s)}{V_Y(s)} = \frac{1}{1+\frac{1}{T(s)}}. \quad (10)$$

For high values of T(s), Av(s) tends towards 1. The CFOA input resistance at the X terminal and the output resistance at the O terminal is approximately given by

$$r_{in-} = r_{out} \approx \frac{(r_{ds14} // r_{ds15})}{T(0)}. \quad (11)$$

The CFOA output resistance at terminal Z is simply obtained as

$$r_Z = r_{ds21} // r_{ds22}. \quad (12)$$

If higher output resistances are needed, cascoded topologies can be used to increase this value and to improve the linearity performance. The CFOA dc open-loop gain can be given as

$$T(0) = \frac{r_Z}{r_{in-} + r_{out}}. \quad (13)$$

III. Simulation Results

The performance of the proposed CFOA circuit was verified by performing PSpice simulations with supply voltages ±0.75 V using 0.25 μm TSMC CMOS technology parameters and transistor aspect ratios given in Table 1. Figure 3 shows the output voltage swing of the proposed CFOA when used to realize an amplifier with different gains. The input voltage was applied at the non-inverting input terminal voltage Y, the output voltage obtained at the O terminal. The inverting input is terminated with 2 kΩ, while the Z terminal is terminated with resistance values of 1 kΩ, 2 kΩ, 4 kΩ, and 8 kΩ. The total standby power dissipation is 0.456 mW. Figure 4 gives the derivative of the output voltage of the proposed CFOA versus the input voltage for different gains. Figure 5 shows the variation of the offset voltage across the X terminal versus the variation in the input current applied across the X terminal (I_X) when V_Y is equal to zero. The X terminal input resistance R_X is less than 36 Ω and the offset voltage is less than 20 mV. Figure 6 shows the Z terminal output current swing versus X terminal input current I_X. Figure 7 shows the magnitude response of the CFOA when it is used to realize a variable gain amplifier, where V_{in} is the AC-varying signal with 1 V magnitude and the inverting terminal is terminated with a 1 kΩ and the Z terminal is terminated with a variable resistance with values of 1 kΩ, 2 kΩ, 4 kΩ, and 8 kΩ. The CFOA shows a constant bandwidth

Table 1. Transistor aspect ratios.

Transistor	W (μm)	L (μm)
M_1-M_4, M_{23}, M_{24}, M_{26}, M_{27}	20	0.25
M_5, M_6, M_{25}, M_{28}	5.25	0.25
M_{10}-M_{13}, M_{32}-M_{35}	140	0.75
M_7 - M_9, M_{29} - M_{31}	113	0.75
M_{18}, M_{14}, M_{21}, M_{38}	294	3.5
M_{16}, M_{17}, M_{36}, M_{37}	1	1
M_{19}, M_{15}, M_{20}, M_{22}, M_{39}	91	3.5

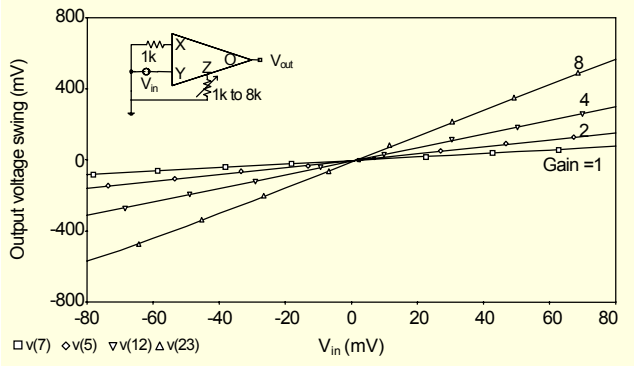

Fig. 3. CFOA-based variable gain amplifier output voltage.

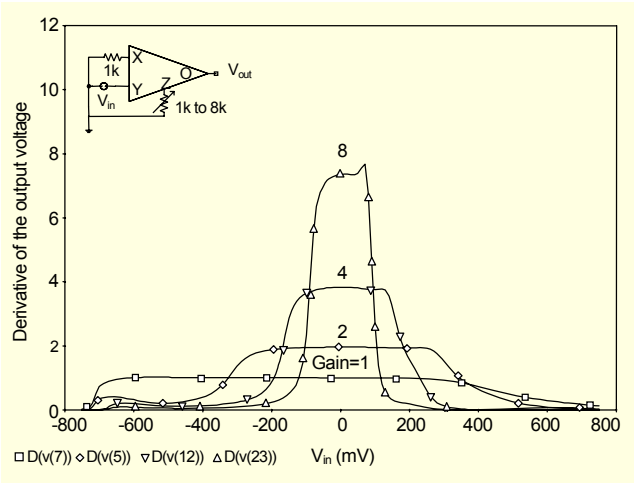

Fig. 4. Derivatives of the output voltage of the proposed CFOA for different gains.

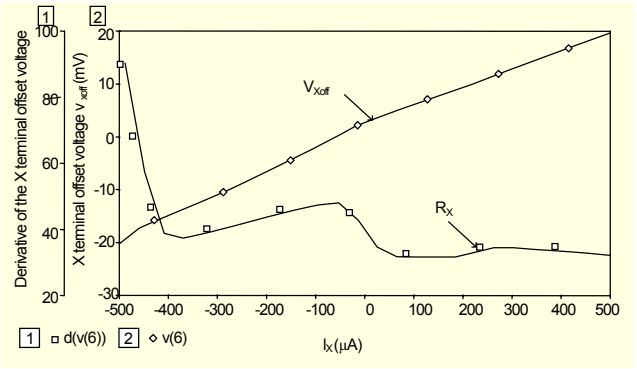

Fig. 5. X terminal offset voltage and its derivative versus X terminal input current I_X.

Table 2. Performance comparison between CFOA introduced in [5], [6], and the proposed CFOA.

Parameters	CFOA [5]	CFOA [6]	Proposed CFOA
CMOS technology (TSMC)	0.5 μm	1.2 μm	0.25 μm
Power supply (V_{DD}, V_{SS})	(2.5 V, -2.5 V)	(1.5 V, -1.5 V)	(0.75 V, -0.75 V)
Total power dissipation	1.25 mW	N.A.	0.456 mW
Input voltage dynamic range	N.A.	-1.4 V to 1.4 V	-0.65 V to 0.65 V
X terminal offset voltage while Y and Z are grounded	N.A.	< 2 mV	< 20 mV
Current driving capability	N.A.	-100 μA, 100 μA	-1 mA, +1 mA
R_X	2 Ω	< 20 Ω	< 36 Ω
CFOA bandwidth	180 MHz	60 MHz	120 MHz

* N.A.= not available

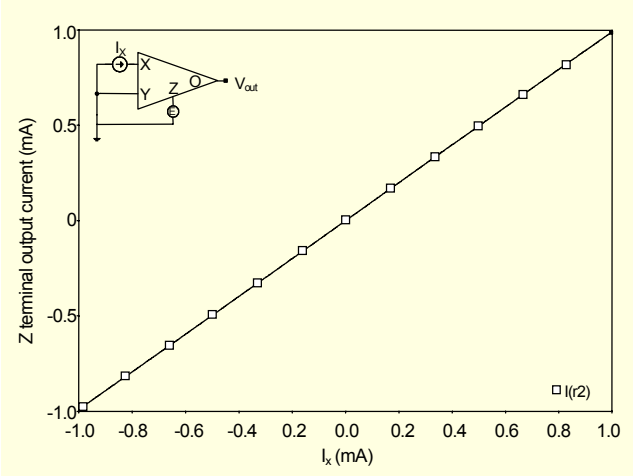

Fig. 6. Z terminal output current swing versus the X terminal input current I_X.

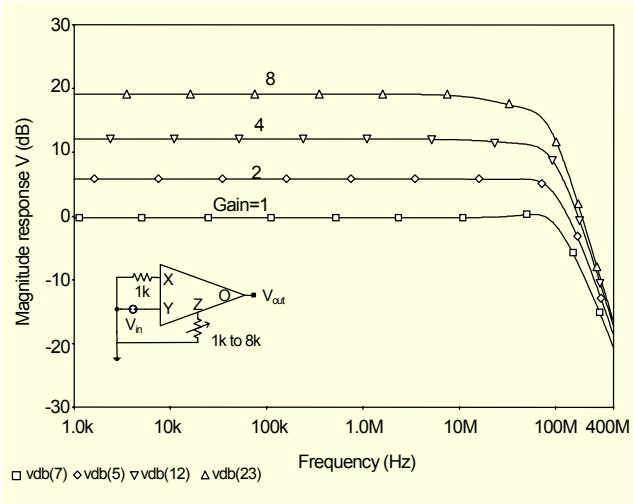

Fig. 7. Magnitude response of the CFOA-based variable gain amplifier.

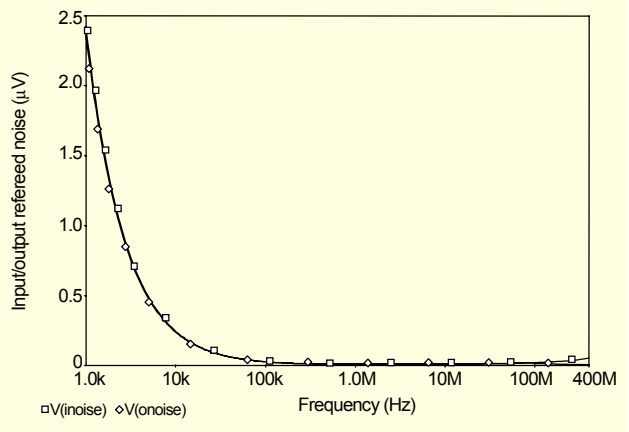

Fig. 8. Input and output referred noise spectral densities.

for different gains. The CFOA has a 3 dB bandwidth of 120 MHz and a phase margin of 68°. The input and output referred noise spectral densities shown in Fig. 8 are less than 2.5 $\mu V/\sqrt{Hz}$. The power supply rejection-ratio (PSRR) from the positive supply to the output is 84 dB, and from the negative supply to the output is 89 dB. Table 2 gives a performance comparison between the CFOA introduced in [5], [6] and the CFOA proposed in this paper.

IV. Application: New CFOA-Based All-Pass Filter

The proposed CFOA is used to realize a new second-order all-pass filter structure which is shown in Fig. 9. The filter consists of three cascading blocks: a weighted differential voltage integrator, a weighted differential voltage adder integrator, and a weighted differential voltage adder amplifier. By cascading the differential voltage adder integrator (N-1) times, an N-order all-pass filter can be realized. By direct analysis, the following transfer function is obtained:

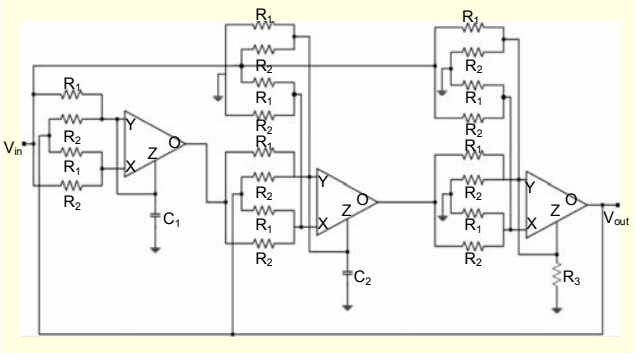

Fig. 9. Proposed CFOA-based grounded-C second-order all-pass filter.

$$\frac{V_{out}}{V_{in}}=\frac{R_3(R_2-R_1)}{R_1R_2}\cdot\frac{s^2-s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)}{s^2+s\left(\frac{1}{C_2}\frac{(R_2-R_1)}{R_1R_2}\right)+\left(\left(\frac{1}{C_1C_2}\right)\left(\frac{(R_2-R_1)}{R_1R_2}\right)^2\right)}. \quad (14)$$

From (14), the ω_o, Q, and DC gain H of the filter are given by

$$\omega_o=\frac{(R_2-R_1)}{R_1R_2\sqrt{C_1C_2}}, Q=\sqrt{\frac{C_2}{C_1}}, \quad H=\frac{R_3(R_2-R_1)}{R_2R_1}. \quad (15)$$

Figure 10 shows the ideal and simulated magnitude and phase responses of the second order all-pass filter given in Fig. 7, where R_2 =20 kΩ, R_1=10 kΩ, R_3=20 kΩ, and C_1=C_2= 0.005 nF.

V. Conclusion

A new CMOS CFOA was presented, analyzed, and simulated. This CFOA has been demonstrated to improve the input stage open-loop bandwidth and reduce the voltage-transfer error. The CFOA block is suitable for low-voltage, low-power applications and is characterized by low voltage-transfer errors and high-output driving current capability. An application example realizing the proposed second-order all-pass filter was given. Table 2 gives a summary of the simulation results and a favorable comparison between the proposed CFOA and the CFOA which was introduced in [5] and [6].

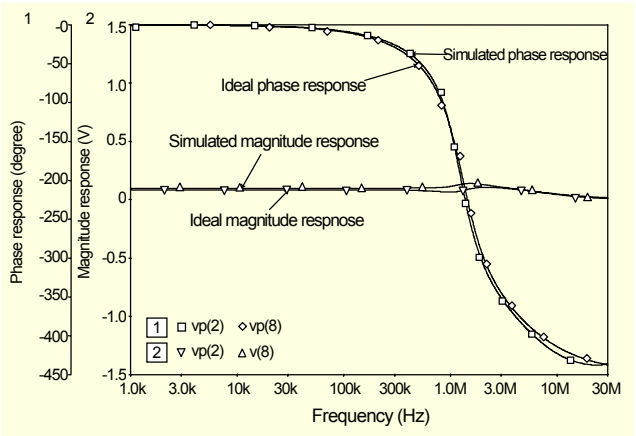

Fig. 10. Ideal and simulated magnitude and phase responses of the second-order all-pass filter based on the proposed-CFOA.

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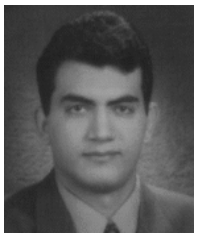

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