Fayoum University

Engineering Faculty

Electrical Engineering Department

B.Eng. Final Year Project

Memristor-based Applications

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June – ٢٠١٦

ACKNOWLEDGMENT

It’s really difficult to show enough gratitude for all those who stood by us to complete our first work and submit our papers in an acceptable forum. We would like to mention Dr. Ahmed Radwan who was there during every step, nothing of this work would have been done without his infinite support. Special thanks to one of the geniuses of EGYPT today, Eng. Mohammed Fouda for his significant advice and help. We are also very thankful for NILE University for their hospitality and devoting all their facilities for anybody in the research field.

Needless to say, we can’t express all the suitable feelings for the one who made us into the Electronics field in the first place, Dr. Rania Fouad Ahmed, our teacher and our supervisor. If,after graduation, we are able to be one tenth of what she is now, we’d be forever grateful and happy.

Our dearest thanks to all the stuff of the electrical department who taught us over the last four years. We looked up for you, and we hope one day we put the name of university high.

DECLARATION

I hereby certify that this material, which I now submit for assessment on the programme of study leading to the award of Bachelor of Science in *Electrical Engineering* is entirely my own work, that I have exercised reasonable care to ensure that the work is original, and does not to the best of my knowledge breach any law of copyright, and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

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ABSTRACT

This book introduces new proposed memristor-based applications. Chapter one begins with a brief introduction about memristor. Chapter two discusses mathematical analysis for series and parallel memristor networks. In chapter three, we try to construct a VCO with simpler relation where we reach a quadratic one. Chapter four proposes new designs for A/D and D/A circuits. The book ends with chapter five where memristor-based PWM circuits are discussed. All circuits are memristor-based and accompanied with appropriate mathematical analysis and simulation results.

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LIST OF ACRONYMS/ABBREVIATIONS

A/D	Analogue to digital
C	Capacitor
CMOS	Complementary metal–oxide–semiconductor
D/A	Digital to analogue
DC	Direct current
HP	Hewlett Packard
L	Inductor
LSB	Least significant bit
M_1	Memristor number one
MSB	Most significant bit
PWM	Pulse width modulation
PVT	Process, voltage and temperature
RF	Radio frequency
TEAM	Threshold adaptive memristor model
TiO_2	Titanium dioxide
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier

Chapter One

١ INTRODUCTION

Before ١٩٧١, only nine types of two-terminal (five passive and four active) elementswere required tomodel any electrical component or circuit. Each elementwas definedby a relation between the state variables of the network: current I, voltage V, chargeQ, and flux ϕ.The relation between these variables is deduced from Faraday's law of induction. A resistor is defined by the relationship between voltage v and current i (dv = Rdi), the capacitor is defined by the relationship between charge q andvoltage v (dq = Cdv), and the inductor is defined by the relationship between flux ϕand current i (dϕ = Ldi). In addition, the current i is defined as the time derivativeof the charge q and according to Faraday's law, the voltage v is defined as the timederivative of the flux ϕ. This relation is shown in Fig.١-١. Leon Chua predicted the existence of the fourth kind of element and called it memristor Fig.١-٢.[١]

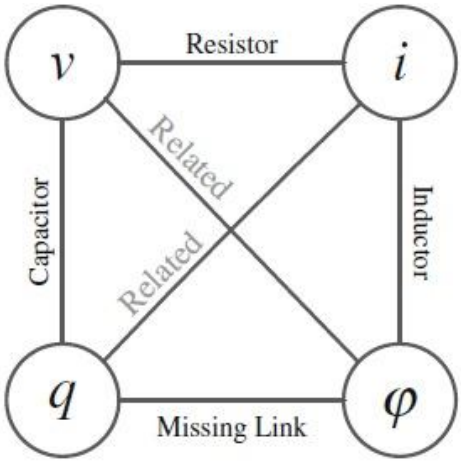

Fig.١-١ The missing link betweencharge and flux.

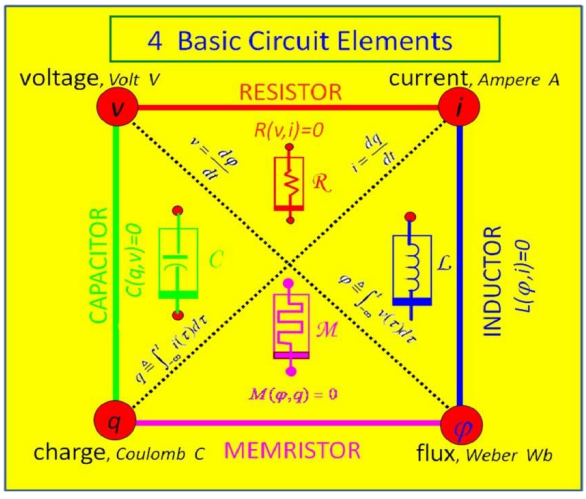

Fig .١-٢ Memristor filled the missing link.

١.١ HP MEMRISTOR

In ٢٠٠٨, Hewlett Packard labs (i.e. HP) announced thatthey found the missing element and published their findings in Nature [٢] and they introduced the first basic model of memristor which is governedby the mathematical formulation of Chua's memristive systems.The HP memristor was built based on titanium dioxide, which is a stable compound.Thememristor structure is composed of two chemically different layers;TiO_2 (high impedance) adjacent to the molecules, and closer to the top platinum electrode,the titanium dioxide was missing around ٢.٥% of its oxygen which is calledoxygen-deficient titanium dioxideTiO_{2-x} (conductive).The oxygen vacanciesare donors of electrons, so the vacancies are positively charged as in Fig.١-٣. When applying a positive voltage to the top electrode of the device, it will repel theoxygen vacancies in theTiO_{2-x} layer (doped region) into the pure TiO_2 (undoped region) which in return will increase the width of TiO_{2-x} and decrease the width of TiO_2. Applying a negative voltage will do the opposite that it will the undoped layer wider and decreases the dopedlayer.

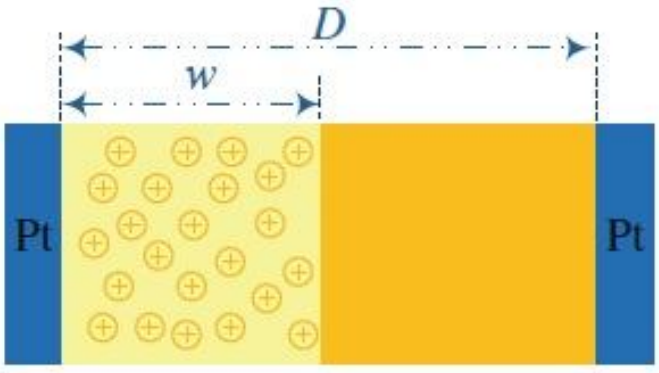

Fig. ١-٣ HP memristor

The HP memristor mainly consists of two series resistors R_{on} and R_{off} which are the resistances of the doped and undoped region respectively. So assuming memristor width is D and the width of the doped region is$w$, the HP mathematical model is

$$M(t) = R_{on}\frac{W(t)}{D} + R_{off}(1 - \frac{W(t)}{D}) \qquad (١.١a)$$

$$\frac{dw}{dt} = \frac{\mu_v R_{on}}{D} i(t) \qquad (١.١b)$$

Where μ_v is the average ion mobility.

١.٢ MEMRISTOR MODEL

In ٢٠٠٨, the first practical model was described by HP labs then later several models were proposed. The most significant models are:

١) The linear ion drift model.

٢) The nonlinear ion drift model.

٣) Simmons tunnel barrier model.

٤) Threshold adaptive memristor model (AKA TEAM model).

Table ١-١ summarizes those models with the appropriate design parameters and symbols [١].

Table ١-١ Different memristor models

Model	Current-Voltage relation	State Variable derivative
Linear ion drift	$v(t) = \left(R_{on}\frac{W(t)}{D} + R_{off}\left(١ - \frac{W(t)}{D}\right)\right)i(t)$	$\frac{dw}{dt} = \frac{\mu_v R_{on}}{D} i(t)$
Nonlinear ion drift	$i\,(t) \;=\; w^n(t)\beta sinh(\alpha v(t)) \;+\; \chi[exp(\gamma\, v(t)) \;-\; ١]$	$\frac{dw(t)}{dt} = a v^m(t)\, f\,(w)$
Simmons tunneling barrier	$i(t)$ $= \tilde{A}(x, vg)\varphi١(vg, x) \times exp\left(-B(vg, x) \cdot \varphi١٫٥(vg, x)\right)$ $- \tilde{A}(x, vg)\left(\varphi١(vg, x) + e\middle\|vg \times exp(B(vg, x)(\varphi١(vg, x) + evg)^{٠٫٥}\right)$ $v_g \;=\; v \;-\; i(t)R_s$	$\frac{dx(t)}{dt} =$ $c_{off} sinh\left(\frac{i}{i_{off}}\right) exp\left[-exp\left(x - \frac{a_{off}}{w_c} - \frac{\|i\|}{b}\right) - \frac{x}{w_c}\right]\; i > ٠$ $c_{on} sinh\left(\frac{i}{i_{on}}\right) exp\left[-exp\left(x - \frac{a_{on}}{w_c} - \frac{\|i\|}{b}\right) - \frac{x}{w_c}\right]\; i < ٠$
Team	$v(t) \;=\; [R_{on} \;+\frac{R_{OFF}-R_{ON}}{x_{off}-x_{on}}(x \;-\; x\_on)].\, i(t)\, or$ $v(t) \;=\; R_{ON}.\, exp(\frac{\lambda}{x_{off}- x_{on}}(x - x_{on})).\, i(t)$	$\frac{dx(t)}{dt} = \begin{cases} k_{off}\left(i(t) i_{off} - ١\right)^{\alpha_{off}} . f_{off}(x) & ٠ < i_{off} < i \\ ٠ & i_{on} < i < i_{off} \\ k_{on}(i(t) i_{on} - ١)^{\alpha_{on}} . f_{on}(x) & i < i_{on} < ٠ \end{cases}$

١.٣ WINDOW FUNCTIONS

Each model has a certain region which can work entirely. For example, the linear ion drift model can work only in the interval of [٠, D]. So to prevent the state variable from getting out of the bound, and also to add more nonlinear behaviour close to the bounds, the derivative of the state variable is multiplied by a window function. So, the window functions should give two things; (١) a state variable working interval, and (٢) the nonlinearity near boundaries to force it to reach zero when the state variable is at the bounds. The different types of window functions are shown in the following table.

Strukov et al. proposed a simple window function that reaches itsmaximum at thecentre of the device, and decreases toward the boundarieswhere it will reach zero speed at the terminal states. This function has a symmetric behaviour which does not describethe real nonlinearities of the memristor.

The most important type that we would use in our work through this book is Biolek window function. Biolek et al. introduced a window function with a solution for the modelling inaccuracy of Joglekar's window function and introduced the first PSPICE model forthe memristor.This SPICE model is most commonly used to simulate thememristor in analogue and digital circuits' ideas.

Also the TEAM window function is designed to fit the behaviour of Simmon tunnel model barrierThere are two functions for ON and OFF switching and do not have to be equallike the Simmons tunnel barrier model where the dependence on X is asymmetric. Theparameters X_{on},X_{off},and W_c are fitting parameters.

Table ٢-٢ Different window functions

	Joglekar[٣]	Biolek[٤]	Prodromakis[٥]	Piecewise[٦]	TEAM[٧]
$\boldsymbol{f(x)}$	$١-(٢x-١)^{٢p}$	$١-\left(x-stp(-i)\right)^{٢p}$	$j(١-\left[(x-٠.٥)^{٢}+٠.٧٥\right]^{p})$	$\begin{cases}\left(١+\left(\frac{x-٠.٥}{a}\right)^{٢b}\right)^{-١} & x_{.} \le x \le ١-x_{.} \\ kx(١-x) & otherwise\end{cases}$	$\exp\left[-exp\left(\frac{\lvert x-x_{on,off}\rvert}{w_c}\right)\right]$
Symmetry	Yes	Yes	Yes	Yes	Not necessarily
Boundaryconditions	No	Discontinuities	Practically yes	Practically yes	Practically yes
Non-linear drift	Partially	Partially	Partially	Partially	Yes
Scalable factor	No	No	Yes	Yes	No
Memristor model	Linear /Non-linear Ion drift /TEAM	Linear /Non-linear Ion drift /TEAM	Linear /Non-linear Ion drift /TEAM	Linear /Non-linear Ion drift /TEAM	TEAM for Simmons tunneling barrier fitting

١.٤ MEMRISTOR-BASED APPLICATIONS

The memristance qualities and operation opened a new track for the implementation of faster and of course much smaller devices, for various applications such as nonlinear analogue circuit design, chaotic systems, non-volatile memory, and neuromorphic systems.

١.٤.١ Memristor-based Oscillators

The oscillators are based on the capacitor as the main component, it uses the charging and discharging of the capacitor as a way to reach two specific levels of voltage, between which, the output waveform would swing. Of course, there're some drawbacks for using capacitors on chips, like size and temperature. Proposing suitable circuits using only memristors and some gates for triggering, we can get an oscillator depending on the change of the value of memristance and hence, the value of voltage across it.

١.٤.٢ Programmable analogue circuits

In many analog circuits such as amplifiers and filters, resistors need to be programmed for adaptation to particular applications or for compensation of PVT (Process, Voltage, and Temperature) variations. The programmable resistor with fine resolution and small parasitic is very useful in many analog and RF range differential circuits. By using the programmable resistance, it can be adopted for programmable attenuators, programmable gain amplifiers and programmable filters, among others.

The traditional method is to use switch-controlled resistors composed of an array of weighted resistors and switches, which would of course introduce much parasitic capacitance and size. Again, the memristor here has an upper hand, it implements the programmable resistor with really tiny size and just small parasitic.

For example, several papers introduce variable-gain amplifier using the memristance, The TiO_2 solid-state memristor was employed in the feedback branch of an inverting voltage amplifier and was programmed externally so the typical circuit gain is M/R_1 followed by a low-pass filter to remove the DC voltage[٨-١٠].

١.٤.٣ Neuromorphic circuits

A neuromorphic system is a mixed mode analog–digital system mimicking neural architecture to pattern neurons by real-time computation, simulation, and emulating the nervous system. But to simulate neural networks in electronic regime neurons and, this requires an implementation with very low power consumption. Electronic synapses are more difficult to engineer as they require being flexible as well as dynamic with memory capability. Thus, the memristor plays a significant role to perform as a synapse with negligible power thrust. And it have been designed a memristor emulator which shows associative memory function with three electronic neurons connected by two memristor–emulator synapses.

١.٤.٤ Chaotic system

Because of the random nature of chaotic systems, the memristor as a nonlinear element is well applicable for encryption and random number generation. The memristor makes it possible for better control and simpler versions of chaotic systems. Chua modelled the memristor to produce a chaotic attractor with negative conductance and capacitor.

After all, we can deduce and say it loud, that memristors opened a new whole opportunities for thinking and trying to reach from good to great, MoNETA, a mind made from memristors would be a great example on the size of efforts and resources dedicated to the research field focusing on applications of memristance, the goddess of memory is now the future of artificial intelligence with all the potentials it still has to introduce.

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Chapter Two

٢ MEMRISTOR NETWORKS MATHEMATICAL ANALYSIS

Before heading towards the applications, memristor shall be studied mathematically first which is the purpose of this chapter,and after a well understanding of that behavior in the very basic networks(i.e. series and parallel networks.), there will be a goodspace for designers to postulate new applications to make use ofthat behavior. The behavior of memristor in a series networkwas already discussed in [١] with two memristors so, dependingon that work;a general formula for n-connectedmemristors either in series or in parallel networks shall be derived withsufficient mathematical conditions. A special case of two-connected memristors is highlighted for the following applications. An emulator for the two series-connected memristors is also represented.

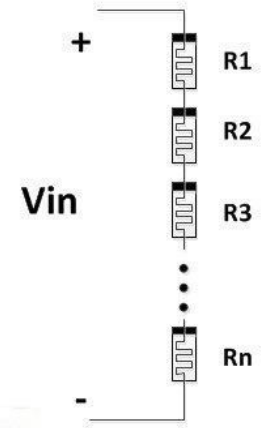

Fig. ٢-١ n series-connected memristors

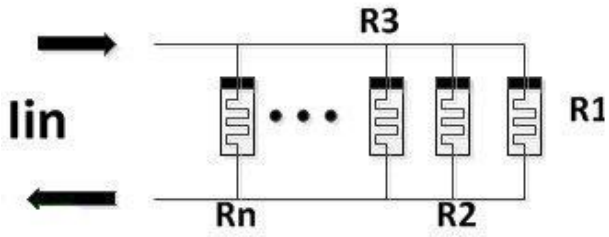

Fig.٢-٢ n parallel-connected memristors

٢.١.١ General behaviour of i^{th} Memristor in n series-connected Memristors

In general, for a current-controlled Memristor

$$\frac{dR_i}{dt} = K_i' i_{in}(t) \qquad (٢\text{-}١)$$

Where$K_i' = -k_i R_d\ (\Omega^{٢} V^{-١} s^{-١})$, $R_d = R_{off} - R_{on}$ for $١ \le i \le n$

Therefore for another memristor j

$$\frac{dR_j}{dt} = K_j' i_{in}(t) \qquad (٢\text{-}٢)$$

From the last two equations it's observed that

$$\frac{dR_j}{dt} = \alpha_{ji} \frac{dR_i}{dt} \qquad (٢\text{-}٣)$$

Where$\alpha_{ji} = \frac{K_j'}{K_i'}$

Integrating both sides of equation (٢-٣) with respect to time

$$R_j(t) = \alpha_{ji} R_i(t) + R_{ind\,ji} \qquad (٢\text{-}٤)$$

Where $R_{ind\,ji} = R_{in\,j} - \alpha_{ji} R_{in_i}$

Working for the i^{th}memristor by substituting for $i_{in}(t)$ in (١-١) as follows

$$\frac{dR_i}{dt} = k_i' * \left(\frac{v_{in}}{\sum_{k=١}^{n} R_k(t)}\right) \qquad (٢\text{-}٥)$$

Substituting from (٢-٤) into the summation of (٢-٥)

$$\frac{dR_i}{dt} = k_i' * \left(\frac{v_{in}(t)}{R_i(t)[\sum_{k=١}^{n} \alpha_{ki}] + [\sum_{k=١}^{n} R_{ind\,ki}]}\right) \qquad (٢\text{-}٦)$$

Organizing last equation

$$(R_i(t)[\textstyle\sum_{k=١}^{n} \alpha_{ki}] + [\sum_{k=١}^{n} R_{ind\,ki}]) * dR_i = k_i' v_{in}(t)\, dt \qquad (٢\text{-}٧)$$

Integrating L.H.S from R_{ini} to R_i and R.H.S from ٠ to t for the last equation

$$[R_i^{٢} - R_{ini}^{٢}] \textstyle\sum_{k=١}^{n} \alpha_{ki} + ٢[R_i - R_{ini}] \sum_{k=١}^{n} R_{ind\,ki} = ٢ k_i' \phi(t) \qquad (٢\text{-}٨)$$

Where $\phi(t)$ represents the flux and assuming zero initial flux. Equation (٢-٨) describes the behaviour of the i^{th} memristor with respect to the total voltage across n series-connected Memristors.

٢.١.٢ Analysis for Two series Memristors

Turning to the special case of two series memristors which is very important case for many applications and is used in the next chapters, substituting for $n = ٢$ and $i = ٢$ in (٢-٨) the result becomes

$$(R_{٢}^{٢} - R_{in٢}^{٢})(١ + \alpha_{١٢}) + ٢(R_{٢} - R_{in٢})R_{ind\,١٢} = ٢k_{٢}'\phi(t) \qquad (٢\text{-}٩)$$

Notice that $\alpha_{٢٢} = ١$ and $R_{ind\,٢٢} = ٠$ from their definitions.

A more specified case with very interesting result is the identical two series memristors with opposite polarities [١, ٢] (i.e.$\alpha_{١٢} = -١$ and$R_{ind\,٢} = R_{in١} + R_{in٢}$), so, substituting in (٢-٩)

$$R_{٢}(t) = R_{in٢} + \frac{k_{٢}'\phi(t)}{R_{in١} + R_{in٢}} \qquad (٢\text{-}١٠)$$

It should be noted in (٢-١٠) that the resistance of the memristor changes linearly with the flux of the total input voltage across the network. This result is very important for many applications and will be used in the next chapters to implement the applications.

٢.١.٣ General behaviour of i^{th} Memristor in n parallel-connected Memristors

Following the same procedure for the series case but with the input current to a voltage-controlled memristor;

In general for a voltage-controlled memristor

$$\frac{dR_i}{dt} = \chi_i' v_{in}(t) \qquad (٢\text{-}١١)$$

Where $\chi = k_i R_d (A^{-١} s^{-١})$ and $R_d = R_{off} - R_{on}$ for $١ \leq i \leq n$

Therefore for another memristor j

$$\frac{dR_j}{dt} = \chi_j' v_{in}(t) \qquad (٢\text{-}١٢)$$

From (٢-١١) and (٢-١٢)

$$\frac{dR_j}{dt} = \alpha_{ji} \frac{dR_i}{dt} \qquad (٢\text{-}١٣)$$

Where$\alpha_{ji} = \frac{K_j'}{K_i'}$

Integrating both sides of equation (٢-١٣) with respect to time

$$R_j(t) = \alpha_{ji} R_i(t) + R_{ind\,ji} \qquad (٢\text{-}١٤)$$

Where $R_{ind\,ji} = R_{in\,j} - \alpha_{ji} R_{in\,i}$

Working for the i^{th}memristor by substituting for $i_{in}(t)$ in (٢-١١) as follows

$$\frac{dR_i}{dt} = \chi_i' * \left(\frac{i_{in}}{\sum_{k=١}^{n} \frac{١}{R_k(t)}}\right) \qquad (٢\text{-}١٥)$$

Substituting from (٢-١٤) into the summation of (٢-١٥)

$$\frac{dR_i}{dt} = \chi_i' * \left(\frac{i_{in}(t)}{\sum_{k=١}^{n} \frac{١}{\alpha_{ki} R_i(t) + R_{ind\,ki}}}\right) \qquad (٢\text{-}١٦)$$

Organizing last equation

$$\sum_{k=1}^{n} \frac{dR_i}{\alpha_{ki}R_i(t)+R_{ind_{ki}}} = \chi_i' i_{in}(t)\, dt \qquad (٢\text{-}١٧)$$

Integrating L.H.S from R_{ini} to R_i and R.H.S from ٠ to t for the last equation

$$\int_{R_{ini}}^{R_i} \sum_{k=1}^{n} \frac{dR_i}{\alpha_{ki}R_i(t)+R_{ind_{ki}}} = \int_{0}^{t} \chi_i' i_{in}(\tau) d\tau \qquad (٢\text{-}١٨)$$

Interchanging integration and summation signs

$$\sum_{k=1}^{n} \int_{R_{ini}}^{R_i} \frac{dR_i}{\alpha_{ki}R_i(t)+R_{ind_{ki}}} = \int_{0}^{t} \chi_i' i_{in}(\tau) d\tau \qquad (٢\text{-}١٩)$$

The result becomes

$$\sum_{k=1}^{n} \frac{1}{\alpha_{ki}} \ln \left| \frac{\alpha_{ki}R_i(t)+R_{ind_{ki}}}{\alpha_{ki}R_{ini}+R_{ind_{ki}}} \right| = \chi_i'\, q(t) \qquad (٢\text{-}٢٠)$$

Substituting from (٢-١٤) into the last result

$$\sum_{k=1}^{n} \frac{1}{\alpha_{ki}} \ln \left| \frac{\alpha_{ki}R_i(t)+R_{ind_{ki}}}{R_{ink}} \right| = \chi_i'\, q(t) \qquad (٢\text{-}٢١)$$

Or equivalently

$$\prod_{k=1}^{n} \left[\frac{\alpha_{ki}R_i(t)+R_{ind_{ki}}}{R_{ink}} \right]^{\frac{1}{\alpha_{ki}}} = e^{\chi_i' q(t)} \qquad (٢\text{-}٢٢)$$

Where $q(t)$ represents the charge of the total input current and assuming zero initial charge. Equation (٢-٢٠) describes the behaviour of the i^{th} memristor with respect to the total current to n parallel-connected Memristors.

٢.١.٤ Analysis for two parallel memristors

For two parallel Memristors, the relation between instantaneous resistance and the charge of the input current is given by substituting for $n = 2$ into (٢-٢١)

$$\frac{1}{\alpha_{12}} \ln \left(\alpha_{12} \frac{R_2(t)-R_{in2}}{R_{in1}} + 1 \right) + \ln \left(\frac{R_2(t)}{R_{in2}} \right) = \chi_i'\, q(t) \qquad (٢\text{-}٢٣)$$

Or equivalently

$$\left(\alpha_{12}\frac{R_2(t)-R_{in2}}{R_{in1}}+1\right)\left(\frac{R_2(t)}{R_{in2}}\right)^{\alpha_{12}}=e^{\frac{\chi_i' q(t)}{\alpha_{12}}} \quad (2\text{-}24)$$

Assume using a square wave input current to the network with frequency $2Hz$ and amplitude $1mA, R_{in1}=R_{in2}=1K\Omega, \chi_2'=400\ A^{-1}s^{-1}$ the equation becomes

$$\alpha_{12}^{\frac{1}{1+\alpha_{12}}}R_2(t)=e^{\frac{\chi_2' q(t)}{\alpha_{12}(1+\alpha_{12})}} \quad (2\text{-}25)$$

Figure 2-3 shows the mathematical graph for (2-25) with $\alpha_{12}=1$ (i.e. the two Memristors are identical and connected with the same polarity). It can be observed from the graph that the behaviour is unique in that case; it's piecewise and linear over small ranges of time but the difference between two successive values increases exponentially with time.

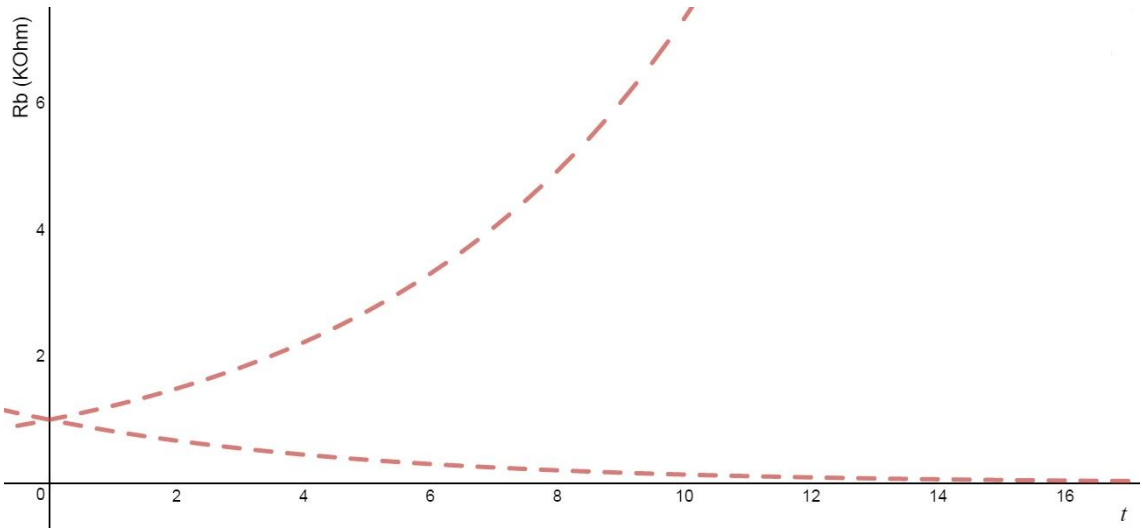

Fig. 2-3 Mathematical graph for memristor behavior to a square wave input current in parallel network

2.1.5 Conditions for two parallel memristors

Constraints can be inspected for a memristor in two parallel-connected memristors from (2-23). It's known that the arguments in the LOG function must be positive and not equal to zero and as the memristor $R_2(t)$ cannot be negative, then the first LOG term in the equation will be of interest, thus

$$1+\alpha_{12}\frac{R_2-R_{in2}}{R_{in1}}>0 \quad (2\text{-}26)$$

Or equivalently

$$\alpha_{12}(R_2 - R_{in2}) > -R_{in1} \quad (2\text{-}27a)$$

Two cases arise from last equation as:

- If$R_2 > R_{in2}$, then the condition becomes

$$\alpha_{12} > \frac{-R_{in1}}{(R_2 - R_{in2})} \quad (2\text{-}27b)$$

- If$R_2 < R_{in2}$, then the condition becomes

$$\alpha_{12} < \frac{-R_{in1}}{(R_2 - R_{in2})} \quad (2\text{-}27c)$$

Figure (2-4) shows the satisfying conditions of (2-27) in the shaded area.

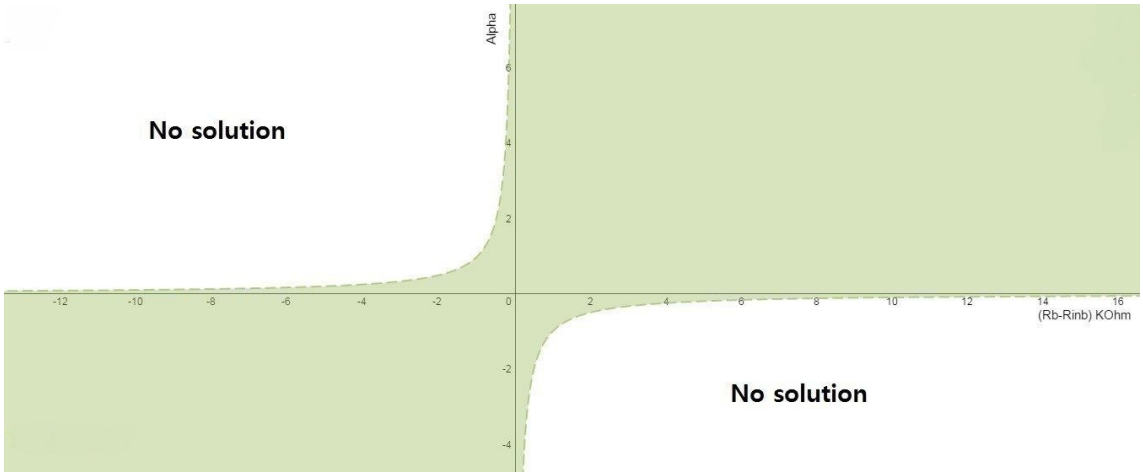

Fig. 2-4 Region of solution of the two parallel-connected memristors

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Chapter Three

٣ VOLTAGE CONTROLLED OSCILLATOR

A key component of many circuits we use today is the VCO, a circuit with an oscillatory output (i.e., sinusoid or other clock signal) whose frequency depends upon an input control voltage. Voltage controlled oscillators (VCOs) are the electronic circuits which are used for high speed clock generation, channel selection, frequency modulation and demodulation in various communication circuits. In the modern communication systems, there is a calculated gap between the adjacent channels for the efficient use of frequency spectrum. Therefore, in order to avoid interference and noise problems, the characteristics of an oscillator are of much importance. Among the compilation of signals, oscillator must be able to detect the desired signal. Hence VCO is a critical component of frequency synthesizer circuits and PLLs. The performance parameters for VCO includes ١) Wide frequency tuning band ٢) Low phase noise ٣) Low power supply noise ٤) Less power dissipation at low supply voltage and small scale technology. Therefore, many researches have been done in this field. Two widely used VCOs are ١) LC oscillators and ٢) Ring VCOs. LC oscillators have better phase noise performance than ring oscillators but the latest trends demand the design with easy implementation of the circuit, small chip area, low cost and good performance. The implementation of high quality inductor and capacitor in a standard CMOS process requires extra non-standard processing steps and also increases the chip area and the cost. On the other hand, ring oscillators are completely integrated circuits. Therefore, the next task is to improve the performance parameters for a ring VCO [١]-[٦]. Still, the size of the integrated circuits is quite large and complicated, so in parallel with trying to improve ring VCO, the magical appearance of memristor had its own opinion to suggest really good applications.

The memristor is used here to replace the capacitor in conventional VCO, its swing between R_{on} and R_{off} acts like charging and discharging of a capacitor, but of course with much smaller area, and very low power consumption.

٣.١ CIRCUIT ARCHITECTURE

The operation of the circuit depends on the oscillation of the resistance of the memristor, which contributes to the output voltage of the circuit with the two values of the high and low outputs.

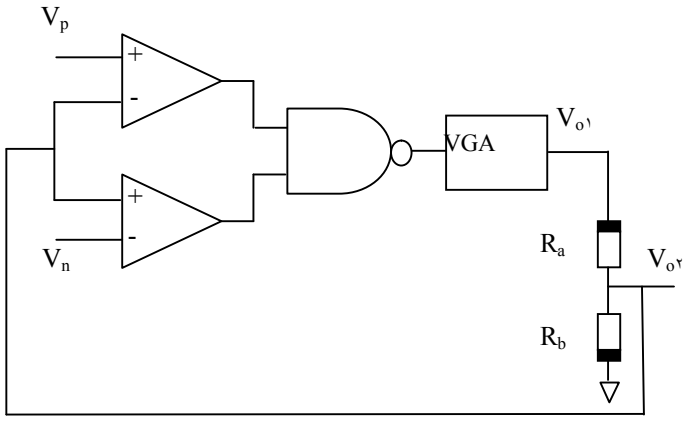

Fig. ٣-١ Memristor-based VCO

The Figure ٣-١ consists of the triggering circuit, the variable gain amplifier and the feedback. The output voltage fed-back to the circuit is extracted from between the two memristors in series, that's why the output voltage is linearly dependant on V_{o1}, the output of variable gain amplifier, the relation for this output voltage can be found in [٧].

Operation of the circuit

This circuit depends mainly on the fact that memristors can tune their values as long as there is some voltage across them. The operation can be simply understood if we considered the waveform of the output and the regions of work for this circuit. Figure ٣-٢ represents the output voltage of the variable gain amplifier as well as the output voltage of the oscillator.

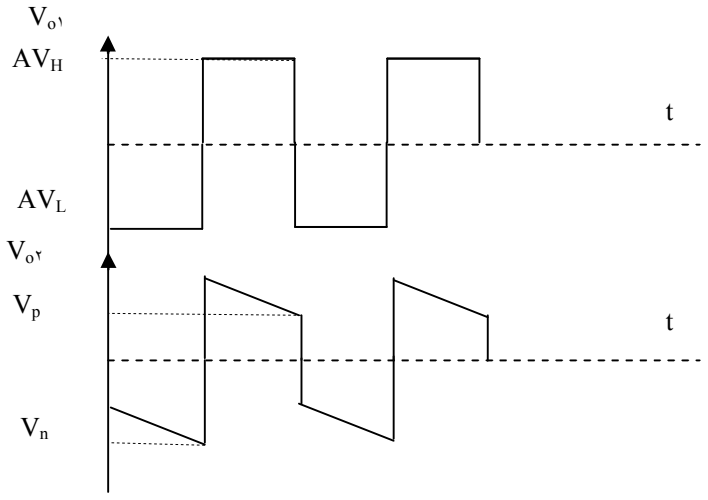

Figure ٣-٢ Output waveform

We have two points the output switches at, V_p and V_n. Starting from zero output, the resulting voltage at the end of the NAND-gate will yield low voltage; which in turn will work on making the memristance R_b higher in value, so the negative voltage across it increases; when it reaches a value of V_n, the voltage at the NAND-gate switches to high which makes the memristance decrease, so will the voltage across it; again the voltage drops below V_p and the output switches to low, and so on.

In our work through this paper we focused on the useful fact that the nonlinearity of the memristance could be eliminated by connecting two memristors with opposite polarity in series and taking the output from the node in between. This again is derived in [٧]. The relation for the memristance in the series case where they have opposite polarity is,

$$R_b(t) = R_{inb} - \frac{k'_m}{R_{ina}+R_{inb}}\varphi(t) \qquad (٣\text{-}١)$$

Where $R_b(t)$ is the memristance of memristor R_b, R_{inb} is its initial value, R_{ina} is the initial value for memristor R_a, $\varphi(t)$ is the flux across the two memristors and $K' = \mu_v R_{on}(R_{off} - R_{on})/D^٢$ which depends on the mobility factorμ_v $(m^٢ s^{-١} V^{-١})$, minimum resistanceR_{on}, maximum resistance $R_{off}$and memristor length D [٧].

٣.٢ ANALYSIS OF THE CIRCUIT

We'll start using the HP general relation [٨],

$$R_a^٢ = R_{ai}^٢ + ٢K' \int_٠^t V_a(\tau)d\tau \qquad (٣\text{-}٢)$$

Where R_a is the memristance of memristor (a) and $V_a(t)$ is the voltage across it.

From which, using differentiation,

$$R_a dR_a = K'(V_{o١} - V_{o٢})dt \qquad (٣\text{-}٣)$$

Similarly,

$$R_b dR_b = K'(-V_{o٢})dt \qquad (3–4)$$

We can now consider the current through each memristor,for memristor R_a,

$$i_a = \frac{V_{o٢} - V_{o١}}{R_a} = -\frac{١}{K'}\frac{dR_a}{dt} \quad (٣\text{-}٥)$$

Similarly for R_b,

$$i_b = \frac{-V_{o٢}}{R_b} = \frac{١}{K'}\frac{dR_b}{dt} \quad (٣\text{-}٦)$$

For ideal comparators with infinite gains,$i_a = i_b$

$$\frac{dR_a}{dt} = -\frac{dR_b}{dt} \quad (٣\text{-}٧)$$

Integrating both sides,

$$\therefore R_a + R_b = R_{ai} + R_{bi} \quad (٣\text{-}٩)$$

This relation shows us clearly that the summation of both memristances is always constant; we will then choose the initial values for the memristances to get the required operation.

We can now try to find the time for each pulse, high and low. Calculating expressions for memristance at switching points, forV_p the voltage at which the output switches to low,

$$V_p = V_{o١H}\left(\frac{R_{bp}}{R_{bi}+R_{ai}}\right) \quad (٣\text{-}١٠)$$

$$R_{bp} = \frac{V_p}{V_{o١H}}(R_{ai} + R_{bi}) \quad (٣\text{-}١١)$$

Where (R_{bp}) is the value of memristance (b) at the switching point, and ($V_{o١H}$) the value of the high output of VGA.And looking for the memristor R_a,

$$V_{o١H} - V_p = V_{o١H}\left(\frac{R_{ap}}{R_{ai}+R_{bi}}\right) \quad (٣\text{-}١٢)$$

$$R_{ap} = \frac{V_{o١H} - V_p}{V_{o١H}}\ (R_{ai} + R_{bi}) \quad (٣\text{-}١٣)$$

ForV_n the voltage at which the output switches to high,

$$V_n = V_{o١L}\left(\frac{R_{bn}}{R_b+R_a}\right) \quad (٣\text{-}١٤)$$

$$R_{bn} = \frac{V_n}{V_{o\text{١}L}}(R_{ai} + R_{bi}) \qquad (٣\text{-}١٥)$$

Where (R_{bn}) is the value of memristance (b) at the switching point, and ($V_{o\text{١}L}$) is the value of the low output of VGA.Again, for memristor R_a,

$$V_{o\text{١}L} - V_n = V_{o\text{١}L}\left(\frac{R_{an}}{R_{ai}+R_{bi}}\right) \qquad (٣\text{-}١٦)$$

$$R_{an} = \frac{V_{o\text{١}L}+V_n}{V_{o\text{١}L}}\ (R_{ai} + R_{bi}) \qquad (٣\text{-}١٧)$$

$$R_{an} = \frac{V_{o\text{١}L}-V_n}{V_{o\text{١}L}}\ (R_{ai} + R_{bi}) \qquad (٣\text{-}١٨)$$

We then use the memristance equations to calculate time,

$$dt = \frac{\text{١}}{K'V_{o\text{١}}}(R_a dR_a - R_b dR_b) \qquad (٣\text{-}١٩)$$

Integrating for high duration and low duration, during the high output, the output voltage is $V_{o\text{١}H}$, hence;

$$T_H = \frac{\text{١}}{\text{٢}K'V_{o\text{١}H}}\left(\left(R_{ap}^{\text{٢}} - R_{an}^{\text{٢}}\right) - \left(R_{bp}^{\text{٢}} - R_{bn}^{\text{٢}}\right)\right) \qquad (٣\text{-}٢٠)$$

For the low output, the reference voltage is $V_{o\text{١}L}$, hence;

$$T_L = \frac{\text{١}}{\text{٢}K'V_{o\text{١}L}}\left(\left(R_{an}^{\text{٢}} - R_{ap}^{\text{٢}}\right) - \left(R_{bn}^{\text{٢}} - R_{bp}^{\text{٢}}\right)\right) \qquad (٣\text{-}٢١)$$

We can then find the frequency of oscillation, which turns out to be calculated as,

$$\therefore f = \frac{K'}{(R_{ai}+R_{bi})^{\text{٢}}\left(\frac{\text{١}}{V_{o\text{١}H}}-\frac{\text{١}}{V_{o\text{١}L}}\right)\left(\frac{V_n}{V_{o\text{١}L}}-\frac{V_p}{V_{o\text{١}H}}\right)} \qquad (٣\text{-}٢٢)$$

For a simple relation we might choose $V_{o\text{١}L}$= -$V_{o\text{١}H}$,

$$\therefore f = \frac{K'}{(R_{ai}+R_{bi})^{\text{٢}}\left(\frac{\text{٢}}{V_{o\text{١}H}^{\text{٢}}}\right)(-V_n-V_p)} \qquad (٣\text{-}٢٣)$$

We know for sure that V_n is a negative voltage and hence;

$$\therefore f = \frac{K'V_{o\text{١}H}^{\text{٢}}}{\text{٢}(R_{ai}+R_{bi})^{\text{٢}}(|V_n|-|V_p|)} \qquad (٣\text{-}٢٤)$$

Where$K' = \mu_v R_{on}(R_{off} - R_{on})/D^2$ depends on the mobility factorμ_v $(m^2 s^{-1} V^{-1})$, minimum resistanceR_{on}, maximum resistance $R_{off}$and memristor length D.

Now, V_{o1H} is the output of the VGA. So, it's actually the output of the NAND gate multiplied by some value (A) which is the gain of the VGA. Hence, we have our final relation; $V_{o1H} = AV_H$

$$\therefore f = \frac{K' A^2 V_H^2}{2(R_{ai}+R_{bi})^2(|V_n|-|V_p|)} \qquad (3\text{-}26)$$

We can now tune our oscillator by adjusting the VGA to get the value of (A) needed to generate our desired frequency.

We can also refer to paper [9], where a voltage-controlled VGA is introduced using the memristors, the relation between the output voltage and control voltage is linear and hence the oscillation frequency we just derived has the same relation with the control voltage without any change.

٣.٣ OPERATION CONDITION

As charges pass through the memristor, the memristance value will change within the range$R_m \in (R_{on}, R_{off})$. Where R_{on} is the minimum memristance above which the resistance of memristor starts to increase and R_{off} is the maximum memristance. So, if this memristance reaches one of its boundaries $R_{on}\ or\ R_{off}$, it will be constant as long as the direction of current doesn't change.Therefore, for a sustained oscillation,R_m should not reach one of the boundaries. In case of reaching one of the boundaries, the output voltage becomes constant.

Thus, the condition for oscillation is,

$$R_{on} < R_{bp} < R_{bn} < R_{off}$$

$$R_{on} < R_{ap} < R_{bp} < R_{off}$$

Using the relations we got earlier for$R_{bp}, R_{bn}, R_{an} and R_{ap}$, we have;

$$V_1 < |V_p| < |V_n| < V_2 \qquad (3\text{-}27)$$

Where,

$$V_{١} = \max\{V_{o١H}\frac{R_{on}}{R_{ai}+R_{bi}}, V_{o١H}\left(١ - \frac{R_{off}}{R_{ai}+R_{bi}}\right)\}$$

$$V_{٢} = \min\{V_{o١H}\frac{R_{off}}{R_{ai}+R_{bi}}, V_{o١H}\left(١ - \frac{R_{on}}{R_{ai}+R_{bi}}\right)\}$$

So, we can choose the values of$V_p$and $V_n$to adjust the levels of switching and the base frequency as well.

٣.٤ SPICE SIMULATIONS

Our simulations are done using SPICE, the model for the used memristor is the one proposed by Biolek with high doping factor $p = ١٠٠$ [١٠]. We used$R_{on} = ١K, R_{off} = ١٠٠K, D = ١٠n$ &$\mu_v = ١٠f$. These values yield$K' = ٩٩٠٠\ M\Omega^{٢}V^{-١}S^{-١}$.

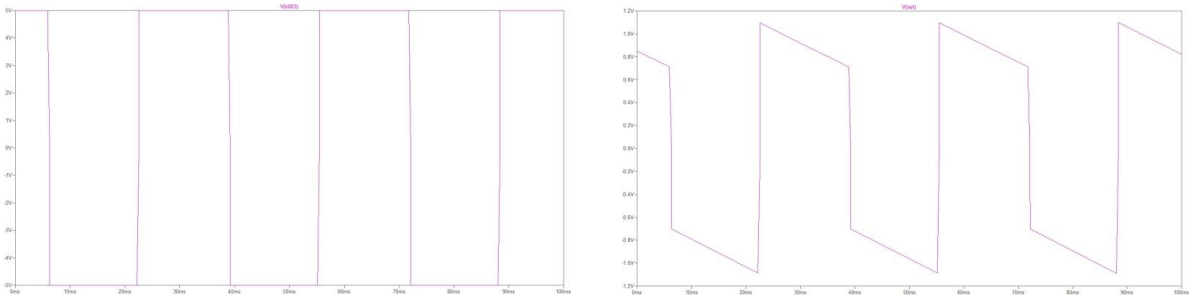

Fig.٣-٣ Simulations using Rai = Rbi = ٥٠K, Vp = ٠.٧V, Vn = -١.١V and AV_H = ٥ V. (a) the AVH waveform. (b) The output voltage on interval of ٠.١ s.

In the figures above, we see that the frequency for the output of VGA of ٥ volt is almost ٣٠ Hz, and it's the same result that can be derived using equation (٢٦).

We've reached a relation that's just simple to have an easy-to-calculate range of frequencies. The design of VCOs using memristors has many advantages; the most noticeable is the low area that comes as a result for replacing enormous reactive components like capacitance and inductance that the current oscillators rely on with very tiny memristor. Also the use of memristors to emulate the VCO is a step toward making use of the new promising technology.

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Chapter Three

٤ CONVERTERS

The cumulative property of the memristor has made a pretty good advancement in the design of many circuits. In this chapter we'll introduce some suggested designs for A/D as well as D/A converters that have really small area and somehow fast enough compared to current available designs.

٤.١ ANALOG TO DIGITAL CONVERTERS

The Digital to analog converters are really important for interfacing the analog and digital domains, they have great potential in modulation of signals as well as demodulation. Along the past decades, many designs have been introduced; each would add the benefit of speed or space above the preceding one.

One of the first examples was based on a switch circuit which consists of all the possible combinations of the input bits [١], it's obvious that the size of the circuit increases enormously for larger number of bits.

There are also the folded resistor-string converters [٢], the circuit depends on a line of series resistors and a decoder that chooses the value according to the bits input. This made the converter faster but with very large decoder introduced. Another design that has a similar problem is the binary weighted resistor converters [٣],it had an idea of making each bit to be represented by a resistor that has a value depends on the position of that bit. Of course the resistors would mount to very large values for higher bits and also they would have noticeably large size on the chip.

Another idea that has been the basis of many designs, is the thermometer-code-based current-mode D/A converter [٤, ٥] which depends on a network of capacitors and transistors. This is obviously having quite large area and doesn't need any further explanation. Some more examples are the resistor-capacitor hybrid converterand the segmented converters [٦, ٧].

After the enormous advance in CMOS technology, and the continuous research for developing faster circuits with transistors having really small sizes, the world witnessed the magical appearance of the memristors in the HP labs [٨].

For the oscillators, the relaxation properties of the memristance made it easier to use the dwarf component as a capacitor; it charges into some memristance value and thenloses it when it's exposed into the same value with the opposite direction [٩].

Also, in digital applications the memristance found its way, starting with half and full adders and through the work on many designs for the memory, the memristor proved to be way faster than conventional CMOS circuits and way much smaller, it's worthy to be mentioned is the paper in [١٠].

Using the memristor in digital to analog converters would be beneficial, it's used to sum the values of the bits, and its size is way smaller than conventional summation circuits using op-amps. The memristor has the ability to perform in various circuits as long as the off-on conditions are maintained.

The main problem is as seen, the size of enormous circuits, and the complexity of the area that increases really fast with the number of bits. In the proposed design each bit is represented with only one transistor, the memristor behavior is fast enough and is expected to have a better behavior over the conventional D/A designs present.

٤.١.١ Unbalanced sizing D/A converter

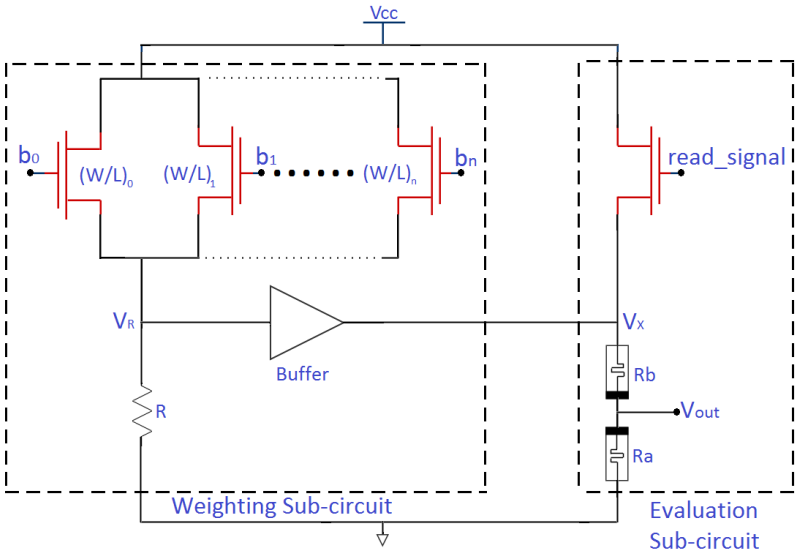

Fig. ٤-١ Proposed circuit for unbalanced sized D/A converter.

Figure ٣-١ shows the proposed circuit where each bit is represented with a transistor, the sizes of the transistors are related to the position of the bits they represents, and the least significant bit has the least sized transistor.The voltage is buffered into two series memristors with opposite polarization. The circuit is considered in two phases, First phase is Pre-charge where the memristor accumulate the voltage from all the bits. Second phase is Evaluation where a very thin pulse is applied to read the value on the memristance with almost no change in its value. After each cycle, a reverse input would delete all what have been done through entering the inverse of each pulse and the reading signal.

The analysis of this circuit can be divided into two major sub-circuits, the first is the weighting circuit that consists of the n transistors that correspond to n bits, the dimensions of the transistors are designed so thatV_x reflects the expected weight of each input bit, the weighting circuit also has a common resistor, and a buffer, this sub-circuit is followed by the evaluationsub-circuit of the memristor where the accumulation occurs. Bits are inserted in serial manner, non-overlapped, although each bit has its transistor, but to get rid of the problem that arises from both transistors being on together, each is inserted in specific time.

Weighting circuit

The analysis is based on the assumption that all the transistors operate in the saturation region, therefore the current through any NMOS transistor can be calculated by:

$$I_{ds} = \frac{١}{٢}\mu.C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^{٢}, \qquad (٤\text{-}١)$$

Where $\mu.C_{ox}$is the trans-conductance, (W/L) is the sizing,V_{gs} is the voltage between the gate and $V_{th}$the source and is the threshold voltage. Since, the voltage at the source node is equal to the voltage across theresistor; it is better to concentrate onthe LSB (least significant bit) and then deduce the sizes of other transistors.

By substituting the voltage at the source with the value needed to represent the LSB, the following relation is given:

$$I_{ds\_LSB} = \frac{١}{٢}\mu.C_{ox}\left(\frac{W}{L}\right)_{LSB}\left((V_g - V_{th}) - V_{LSB}\right)^{٢}, \qquad (٤\text{-}٢)$$

So, the gate voltage which is the input voltage is known, also the value needed to represent the LSB, so by specifying some value for the sizing of the LSB transistor, the value of the current can be calculated.

After that, calculating the value of the resistance needed, simply from elementary circuits,

$$R = \frac{V_{LSB}}{I_{ds\_LSB}} \qquad (٤\text{-}٣)$$

It can also be deducedthat the size of each transistor depends on the weight of each correspond bit which is given by A. For the case of binary, the value of A depends on the position of bit (n), it takes values $A \in \{١, ٢, ٤, ٨, ١٦, \dots\dots, ٢^{k-١}\}, where\ k\ is\ the\ number\ of\ bits$. So the current for transistor (n);

$$I_{ds\_n} = \frac{١}{٢} A\mu . C_{ox} \left(\frac{W}{L}\right)_{LSB} ((V_{cc} - V_{th}) - V_{LSB})^{٢}. \qquad (٤\text{-}٤)$$

And from the transistor current relation,

$$I_{ds\_n} = \frac{١}{٢} \mu . C_{ox} \left(\frac{W}{L}\right)_{n} ((V_{cc} - V_{th}) - AV_{LSB})^{٢}. \qquad (٤\text{-}٥)$$

So, the sizing ratio of all transistorscan be found using the following relation,

$$r = \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_{LSB}} = \frac{A((V_{cc}-V_{th})-V_{LSB})^{٢}}{((V_{cc}-V_{th})-AV_{LSB})^{٢}}. \qquad (٤\text{-}٦)$$

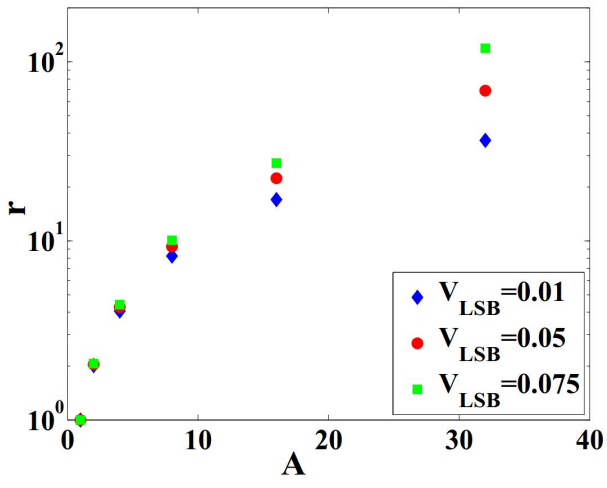

Fig. ٤-٤The dimensions ratio vs. weight

Figure ٣-٢ shows the relationship between the transistors size ratio versus A where the more the LSB voltage is reduced, the less the required sizing becomes.

Evaluation circuit

For two memristance a & b in series with opposite polarities, recalling equation of two series memristors and since input voltage across the combination of the two memristors is constant,

$$\varphi(t) = \int_{.}^{T} V\, dt = VT, \qquad (٤\text{-}٧)$$

Where T is the duration of the input voltage and V is the voltage across the memristor,

$$R_a = R_{ina} + \frac{K'_a VT}{R_{ina}+R_{inb}}. \qquad (٤\text{-}٨)$$

Hence, there are two possibilities to think of, possibility of varying the duration depending on the position of the bit, but it would be quite a problem for the case of many bits and a good way for synchronization would be needed. Also of course, varying the input voltage, which have been done in the proposed circuit using transistors with weight A, and so on. Of course, in the case of many bits huge transistors are required but this could be controlled using combination of sub-circuits from smaller digital to analog converters and varying the initial conditions of the memristors.

So, across the memristance R_a value of total memristance,

$$R_a = R_{ina} + \frac{K'_a T}{R_{ina}+R_{inb}} \sum_{n=.}^{k} b_n A_n V_{LSB}. \qquad (٤\text{-}٩)$$

It's found actually that $R_{ina} + R_{inb}$ is constant value that may berepresented with R_{iM}, or initial memristance, so the final relation,

$$R_a = R_{ina} + \frac{K'_a T}{\mathrm{R_{iM}}} \sum_{n=.}^{k} b_n A_n V_{LSB}. \qquad (٤\text{-}١٠)$$

The voltage across it as an output voltage,

$$V_{out} = I_{read} R_a, \qquad (٤\text{-}١١)$$

Where,

$$I_{read} = \frac{V_{read}}{R_{ina}+R_{inb}}. \qquad (٤\text{-}١٢)$$

From equation (١٠), if the initial memristance is biased to have a very small value and the rest of the parameters of the memristor are adjusted so that the change in the value due to being connected to a voltage with value of the LSB is around the ratio needed for the LSB representation (١/٤ in the case of ٢-bit D/A converter for example).Some sort of an example of how things work is introduced. ٣ bit D/A converter in Figure ٣-٣, a plot of signals over the circuit.

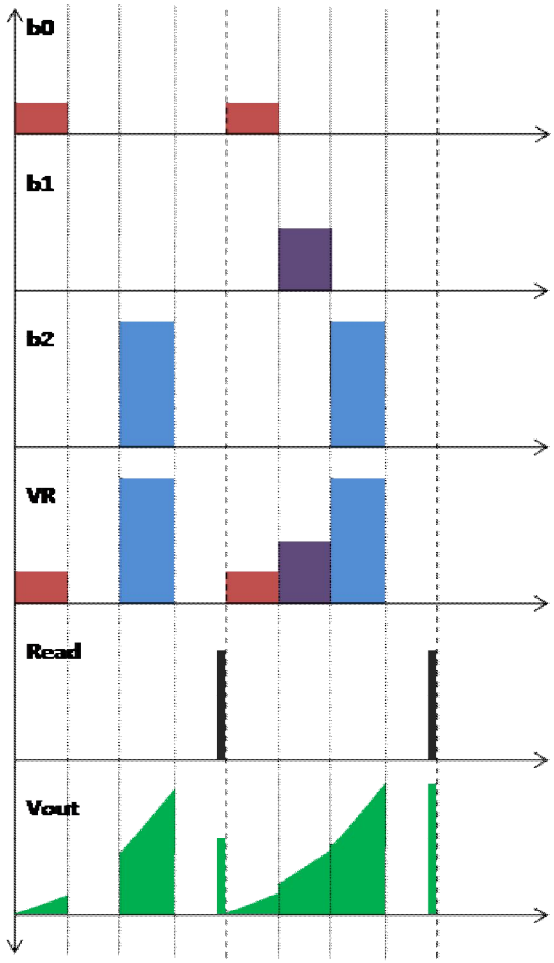

Fig.٤-٣ Three bit D/A example

SPICE simulations

The simulations are carried for the ٢-bit D/A converter, all simulations are done using Spice model, and the model for the used memristor is the Biolek model [١٢], with doping factor $p = ١٠, R_{on} = ١K,\ R_{off} = ١٠٠K, D = ١٠\ n.$ Also, μ_v calculated $٢٥٠f$ these values yield$K' = ٢٤٧.٥\ G\Omega^{٢}V^{-١}S^{-١}$.

The converter is designed following the steps mentioned earlier, parameters of the spice default model are usedfortheNMOS, it has $\mu.C_{ox} = ٢٠\ \mu\ Amps/Volts^{٢}$ and $V_{th} = ٠\ v$. Taking the value for$V_g = ٥v, V_{LSB} = ١v$, and$\left(\frac{W}{L}\right)_{LSB} = ٢$, then using equation (٤-٧) to get$\left(\frac{W}{L}\right)_{MSB} = ٧.١$, also biased$R_{ina} = ١k$ &$R_{inb} = ٩٩k$.

Then, from equation (١١), it can be simply calculated the change in the memristance value, it can be found for the four possible cases as follows,

$$\Delta R_{a\ ٠٠} = ٠$$
$$\Delta R_{a\ ٠١} = ٢٤.٧٥\ K\Omega$$
$$\Delta R_{a\ ١٠} = ٤٩.٥\ K\Omega$$
$$\Delta R_{a\ ١١} = ٧٤.٢٥\ K\Omega$$

Using elementary circuits, a read voltage of ٥ volts will cause an output voltage that mounts to the values of ٠.٠٥, ١.٢٨٧٥, ٢.٥٢٥, ٣.٧٦٢٥ which is very good approximations for the conventional D/A converter which has an error up to$\frac{١}{٢}V_{LSB}$.

The same results are obtained using simulations as shown here in Figure ٣-٤ and Figure ٣-٥ the memristance changeand output of the evaluation circuit for the case {١١}.

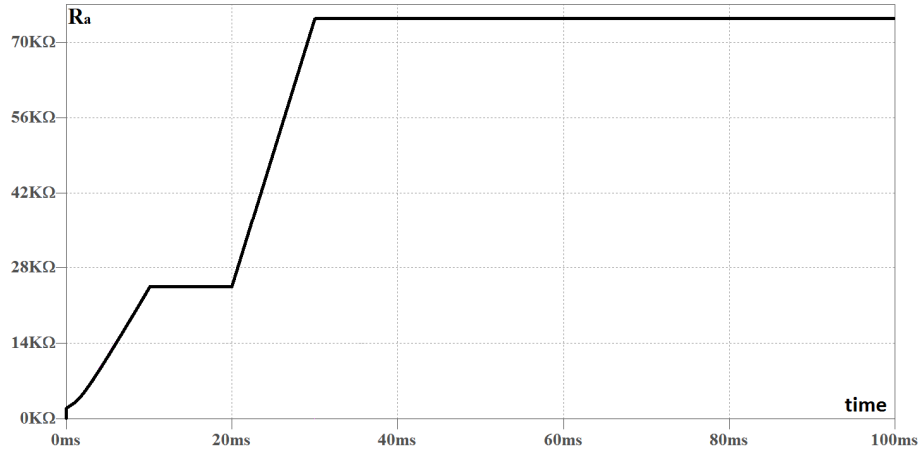

Fig. ٤-٥ Memristance Ra change

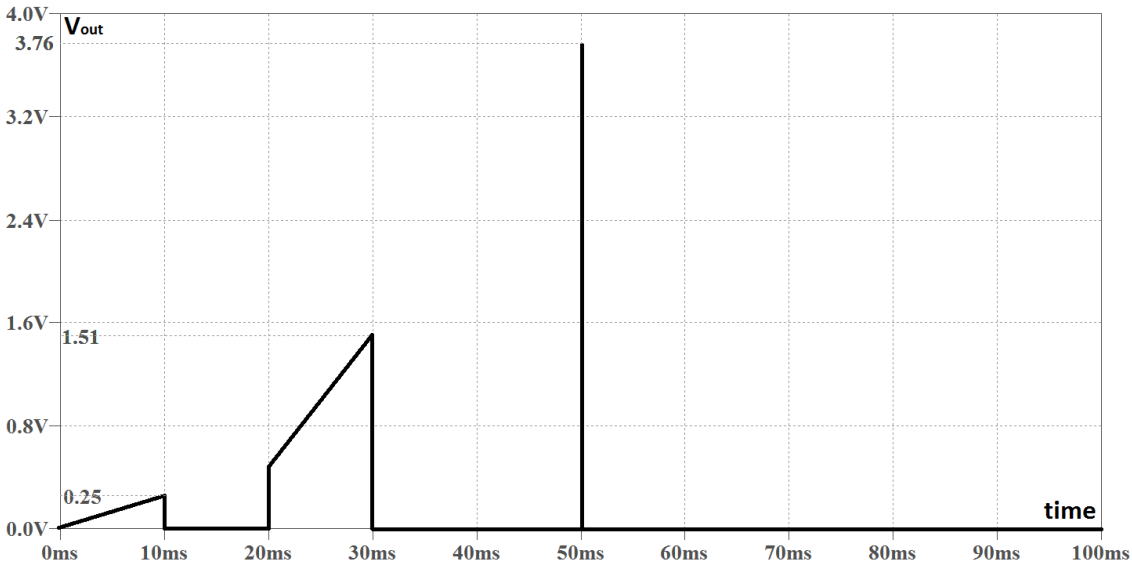

Fig. ٤-٦the output of the evaluation circuit

٤.١.٢ Compensated circuit

The proposed circuit in last section has a kind of obvious disadvantage, the inputs are introduced serially and so, the frequency is scaled down. As a try to give the inputs all together, a more complex circuit with area scaling up really bad with higher number of bits, still, a ٢-bit circuit is introduced as shown in Figure ٤-٦.

The main problem is that when both transistors are on, they work as an equivalent one with dimensions equal the sum of them both; so, compensating the difference in current supplied using two series transistors that'll work only in the case of both inputs are ones might help.

The total equivalent transistor dimensions are easily derived to submit a voltage with weight A = ٣ when both bits are ones,

$$\left(\frac{W}{L}\right)_{overall} = \frac{٣\left(\frac{W}{L}\right)_{LSB}\left((V_g - V_{th}) - V_{LSB}\right)^{٢}}{\left((V_g - V_t) - ٣V_{LSB}\right)^{٢}}, \qquad (٤\text{-}١٣)$$

And so, the compensation transistors required dimensions,

$$\left(\frac{W}{L}\right)_c = \left(\frac{W}{L}\right)_{overall} - \left(\left(\frac{W}{L}\right)_{LSB} + \left(\frac{W}{L}\right)_{MSB}\right). \qquad (٤\text{-}١٤)$$

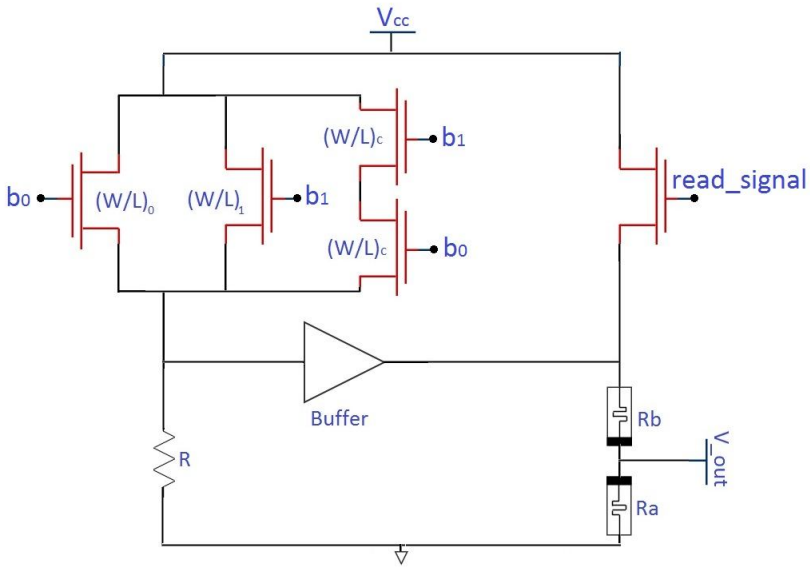

Fig. ٤-٧ Compensated circuit

٤.١.٣ Balanced-sizing circuit

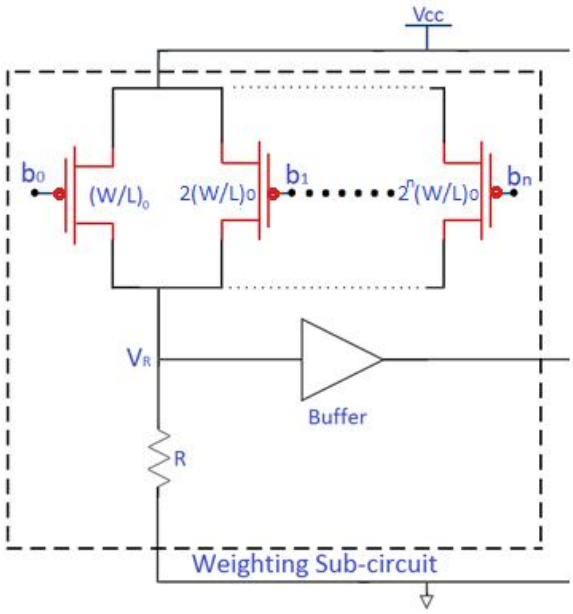

Fig. ٤-٨ Balanced-sizing circuit

The above figure shows the first stage of the balanced-sizing circuit. We'll only consider the first stage in our analysis as the second stage analysis is typically the same as this for the unbalanced circuit.

The whole idea is about reducing the time interval required for the operation of the converter and therefore preserving the frequency. This design is suitable for overlapped bits; we can input all bits in just one cycle, the sizing of the transistors take values from$\{١, ٢, ٤, ٨, ١٦, \dots\dots\dots, ٢^{n-١}\}$, where n is the number of bits.

Now, we prepare the environment for all the transistors to work in the saturation region. We already know the drain current of the PMOS transistor [١٣],

$$I_{ds} = \frac{١}{٢}\mu_{\mathrm{p}} C_{ox} \frac{W}{L}\left(V_{gs} - V_{tp}\right)^{٢} \qquad (٤\text{-}١٥)$$

We therefore can clearly see that $V_{gs}$is constant and all the dependency is upon the dimensions of the transistor; which depends on the weight of the bit that the transistor represents. As the resistor we take the voltage across is constant, from the simple Ohm's law we are sure that the voltages representing each bit are depending on their weight and would take values $\{V_{LSB}, ٢V_{LSB}, ٤V_{LSB}, ٨V_{LSB}, \dots\dots\dots, ٢^{n-١}V_{LSB}\}$.

Limitation on the value of representation voltage

Of course, there's one limitation on the value we would choose for the least significant bit voltage, this limitation arises from the condition imposed on the transistor to work in the saturation region. For any PMOS transistor to work in saturation region it should be achieved that$V_{sd} > V_{sg} - \left|V_{tp}\right|$from which we continue our calculations [١٣],

$$V_d < V_g + \left|V_{tp}\right| \qquad (٤\text{-}١٦)$$

From which we have to be sure that the largest voltage across the resistor follow the relation, and the largest voltage is the most significant bit voltage (MSB). Hence,

$$(١ + ٢ + ٤ + \cdots + ٢^{n-١})V_{LSB} < V_g + \left|V_{tp}\right| \qquad (٤\text{-}١٧)$$

$$V_{LSB} < \frac{V_g + |V_{tp}|}{٢^{n} - ١} \qquad (٤\text{-}١٨)$$

Where$\left(١ + ٢ + ٤ + \cdots + ٢^{n-١} = ٢^{n} - ١\right)$

SPICE simulations

For two-bit D/A converter, we used V_g of ٣V &$V_s$of ٥V, we alsoused ٦٥-nm model for the PMOS, with$V_{tp} = -٠.٢٥\,V$ &$k'_p = ١١٠\ \mu A/V^{٢}$, using equation (٣-١٨), LSB voltage must not exceed value of ١.٠٨٣, and so, we choose$V_{LSB} = ١V$, from which we compute $R = ٢.٩٦٩\ k\Omega$.

The figure ٣-٨ shows the result of the simulations, three periods each of ٠.٥ seconds have the following series of inputs{٠١, ١٠, ١١}.

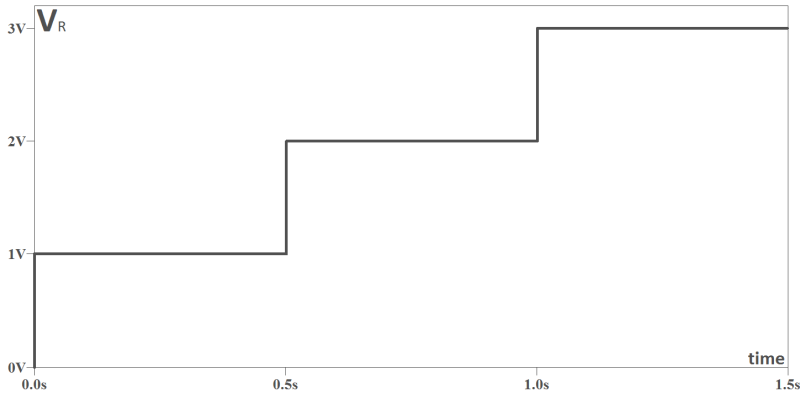

Fig. ٤-٩ Output voltage of the balanced-sizing weighting sub-circuit

The output of the weighting circuit is then buffered into the evaluation circuit where the same approach of the unbalanced-sizing converter is used again. This design saves the clock, every conversion process requires only one cycle instead of n cycles for the unbalanced-sizing design.

This new design of D/A converter has small area, it's faster than conventional designs, the memristor accumulation served in place of many components, weighted resistors or even a huge capacitor, the unbalanced-sizing design introduced a good range for the value of LSB voltage, whereas the balanced-sizing design imposed a limitation, but with a great advantage of clock saving.

٤.٢ ANALOG TO DIGITAL CONVERTER

Needless to say, A/D converters are used in so many circuits in every digital system now, converting the analog signals, the real signals, what we say, what we see, converting continuous signals into digital ones that the modern devices, computers and mobile phones can use and process.

One of the common available A/D converters is a family of integrating converters [١٤]. Integrating A/D converter is a popular approach for realizing high-accuracy data conversion on very slowmoving signals. These types of converters have very low offset and gain errors in addition to being highly linear. A further advantage of integrating converters is the small amount of circuitry required in their implementation. One application that has traditionally made use of integrating converters is measurement instruments such as voltage or current meters. More about conventional A/D converters can be seen in [١٥-١٨].

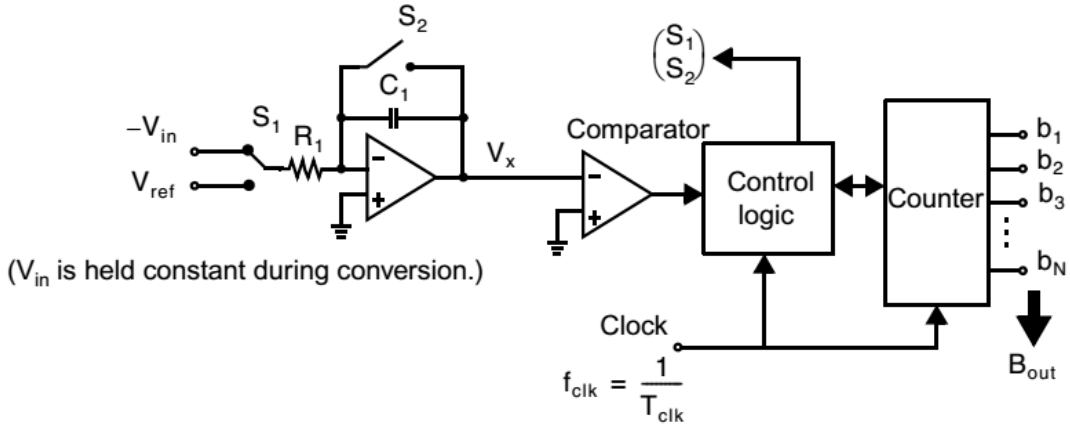

Fig. ٤-١٠ integrating A/D converter

In this section we are to introduce a new design using the memristors, this designs saves a whole lot of area, it doesn't require much logic and it's really simple and easy to analyze. Again, we use the accumulation of the memristance but this time as a ramp, it might be thought of as a replacement for the capacitance with its big on-chip size.

٤.٢.١ Memristor-based A/D converter

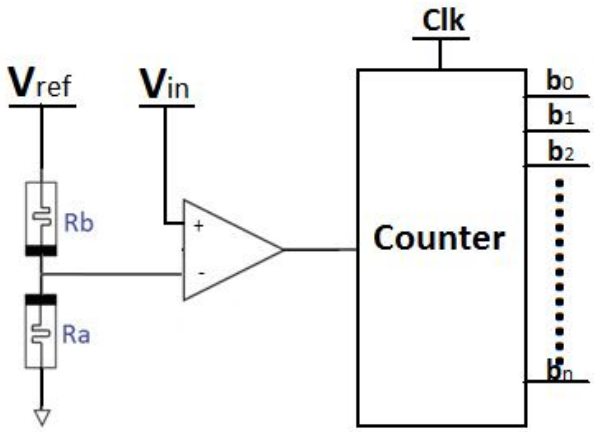

Fig. ٤-١١ Memristor based A/D converter

The circuit shown in the figure ٤-١٠ is a simple circuit of the proposed design. The memristor accumulates until it reaches the off memristance at the full scale input voltage or the maximum possible input voltage. This design depends mainly on the clock of the counter which defines the number of bits this converter can represent.

Analysis & Operation

As always, we took advantage of the linearity of two series memristors, we start our calculations from the relation,

$R_a(t) = R_{ina} + \frac{k'_a}{R_{ina}+R_{inb}}\varphi(t)$ [٩], where V_{ref} is a constant and so, as in equation (٤-٨)

$$R_a = R_{ina} + \frac{K'_a VT}{R_{ina} + R_{inb}}$$

We normally selectR_{ina} small enough not to unnecessarily lose too much time at the boundaries, and hence, we can calculate the time for which the memristor swings betweenR_{on}&R_{off},

$$T_{full} = \frac{(R_{off}-R_{ina})(R_{ina}+R_{inb})}{K'_a V_{ref}} \qquad (٤-١٩)$$

Substituting for$K'_a = \mu\frac{R_{on}(R_{off}-R_{on})}{D^2}$,

$$T_{full} = \frac{(R_{off} - R_{ina})(R_{ina} + R_{inb})}{R_{on}(R_{off} - R_{on})\, D^{٢} V_{ref}} \qquad (٤\text{-}٢٠)$$

So, for n-bits converter all we have to do is to select the clock of the counter, for the same design would work for several n-bits converters depending on the clock we use.

$$T_{Clk} = \frac{T_{full}}{٢^{n}} \qquad (٤\text{-}٢١)$$

Therefore, the output of the comparator is always high and the counter is counting until the value of the voltage across the memristor exceeds that of the input, at this point the output switches to low, and the counter stops counting giving at the end of full-scale time; the result of the conversion.

Before proceeding, it should be noted that when discussing the design of A/D converters, we usually ignore the offset present in the A/D transfer characteristic. Such a simplification is made so as not to complicate the concepts presented.

٤-bit A/D example

Let's consider a ٤-bit converter; we can construct the ranges for the ١٦ possible cases depending on the value of the reference voltage. To make use of this example in the next section let's assume that reference voltage is ٥. We construct a table of ranges and the expected output of the A/D converter in table ٤-١.

We simply divide the reference into number of levels and represent each value with a sequence which is then encoded into bits in the third column.

Range	Value	Bits
٠ – ٠.٣١٢٥	٠	٠٠٠٠
٠.٣١٢٥ – ٠.٦٢٥	١	٠٠٠١
٠.٦٢٥ – ٠.٩٣٧٥	٢	٠٠١٠
٠.٩٣٧٥ – ١.٢٥	٣	٠٠١١

١.٢٥ – ١.٥٦٢٥	٤	٠١٠٠
١.٥٦٢٥ – ١.٨٧٥	٥	٠١٠١
١.٨٧٥ – ٢.١٨٧٥	٦	٠١١٠
٢.١٨٧٥ – ٢.٥	٧	٠١١١
٢.٥ – ٢.٨١٢٥	٨	١٠٠٠
٢.٨١٥ – ٣.١٢٥	٩	١٠٠١
٣.١٢٥ – ٣.٤٣٧٥	١٠	١٠١٠
٣.٤٣٧٥ – ٣.٧٥	١١	١٠١١
٣.٧٥ – ٤.٠٦٢٥	١٢	١١٠٠
٤.٠٦٢٥ – ٤.٣٧٥	١٣	١١٠١
٤.٣٧٥ – ٤.٦٨٧٥	١٤	١١١٠
٤.٦٨٧٥ – ٥	١٥	١١١١

Table ٤-١ ٤-bit A/D converter ranges

SPICE simulations

Simulating the example in the previous section on Spice, we use counter ٧٤HCT١٦١ and the memristor found in Biolek [١٢], with doping factor $p = ١٠, R_{on} = ١٠٠,\ R_{off} = ١٦K, D = ١٠\ n$. Also, $\mu_v = ١٥٠f$ these values yield$K' = ٢.٣٨٥\ G\Omega^{٢}V^{-١}S^{-١}$.

And using$R_{ina} = ٢٠٠$, we calculate the full-scale time$T_{full} = ٢١.١٩٩\ ms$, and therefore, for realizing a ٤-bit A/D converter, we adjust our clock period to $١.٣٢٥\ ms$.

The following figures show the output of the counter for two different cases we considered,

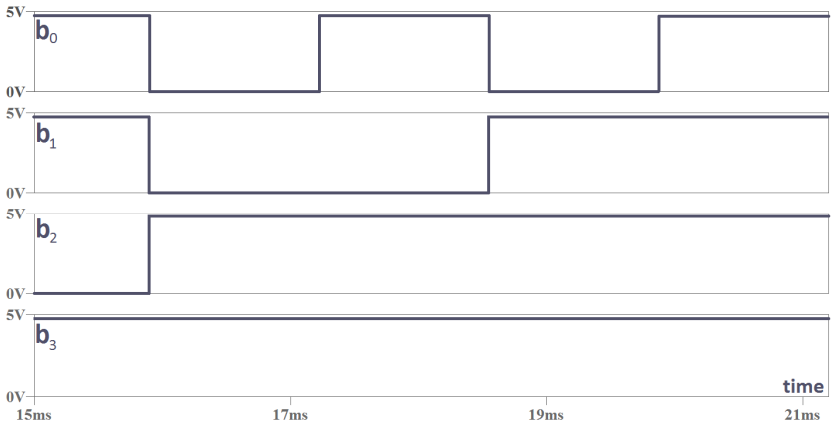

Fig. ٤-١٢ output of converter for input ٤.٨٥ V.

Fig. ٤-١٣ output of converter for input ٣.٨٥ V.

As we notice, we considered the output at the final time after the full-scale time of ٢١.٢ ms, we see that results we computed theoretically and listed in table ٤-١.

We can control the clock and convert the circuit into any number of bits we wish, just we have to be careful that the initial value of memristance should not cause significant shift in the voltage value, the initial value is considered as an offset that can be taken into accounts, and of course minimizing it as possible would give more accuracy.

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Chapter Five

٥ MEMRISTOR-BASED PULSE WIDTH MODULATION

The behaviour of the memristor to current or voltage is of an importance as it's a unique behaviour with respect to resistors that used to be constant and linear in most practical cases. Another feature that makes memristor attractive to researchers and designers is that it has a very small area with respect to other electronic components and it's less power hungry. Because of these reasons, researchers from all over the world have started significant experiments to demonstrate the applications of the memristor. Memristors have been proposed for a wide range of applications such as nonlinear analogue circuit design, chaotic systems, non-volatile memory, and neuromorphic systems [١]. In this chapter, a proposed application of the memristors in the area of designing Pulse-width modulation (PWM) circuits is presented. PWM (also known as pulse-duration modulation) is one of the most important modulation techniques used in communication field when dealing with analogue signals. However, its main purpose is supplied power control to electrical devices such as controlling the speed of a dc motor using microprocessor. The general idea of PWM is to control the width of the output pulse using the input voltage level in a specific time period.

Three cases of PWM can be generated depending on where the output pulse is set with respect to the input sample time period; either lead edge-aligned PWM, tail- edge (trail) aligned PWM, or centre aligned PWM [٢]. The basic idea of using memristors in designing PWM circuits is the relation between memristor behaviour and the base of PWM. The memristor resistance is a function of the voltage level across the memristor [٣]-[٤], also, the PWM output is function of the input voltage level.

An important concept should be taken into account when dealing with memristor is called resetting mechanism [٥]. This concept states that because the memristor changes its state over time (i.e. the dynamic nature of memristor), the reverse of the signal should be entered every cycle to reset the memristor to its initial state and to ensure continuation of the process (i.e. to prevent the memristor from reaching its boundaries and to work in the same range every cycle).

This chapter introduces simple PWM circuits based on memristors to generate the three cases of the PWM. The proposed circuits compose of two main parts; a pre-modulation circuit to confirm the resetting concept and a modulation circuit to perform the PWM. The chapter is arranged as follows; section ٥.١ describes the pre-modulation circuit. The proposed circuits for the three PWM cases are presented in sections ٥.٢, ٥.٣ and ٥.٤. An enhanced design for the centre case is further discussed in ٥.٥.

٥.١ PRE-MODULATION CIRCUIT

٥.١.١ Circuit description

Figure ٤.١, shows the fundamental block diagram for modulation circuit that ensures resetting mechanism via a pre-modulation circuit to prepare the input signal for modulation.

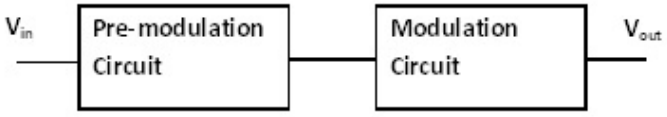

Fig. ٥-١ Block diagram for PWM circuit

The main purpose for the pre-modulation circuit is the clearance of memristor every cycle, therefore, each sample time should be divided equally between the sampled input signal and its inverse polarity. Figure ٥.٢ shows the basic circuit diagram for the pre-modulation circuit.

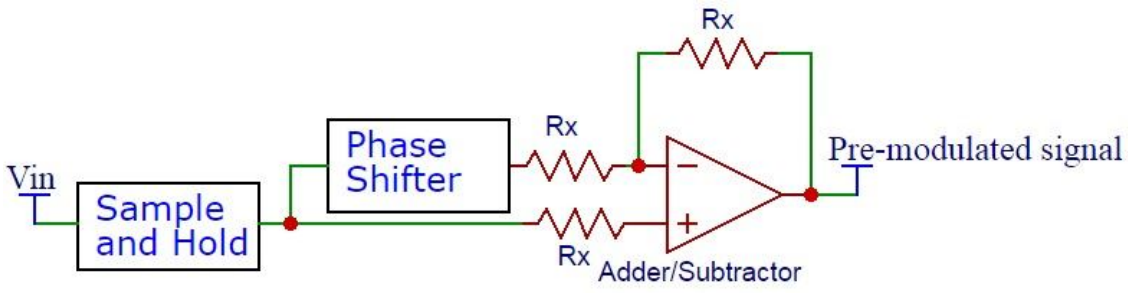

Fig. ٥-٢ Basic pre-modulation circuit diagram

٥.١.٢ Operation mechanism

First, the input signal is sampled by means of sample-and-hold circuit. Then, shifted using a shifter circuit and finally subtracted from its original version via an Adder/Subtractor circuit. This ensures that the sampled signal and its negative exist each cycle. The shift produced by the shifter circuit must be half the sample period which is a condition for producing proper pre-modulated signal. Figure ٥-٣, shows the SPICE simulation output of the pre-modulation circuit for sinusoidal input signal with ١ Hz frequency. It should be mentioned that modifying the pre-modulated signal to be flat-top is recommended to ensure a stable behaviour of the memristors.

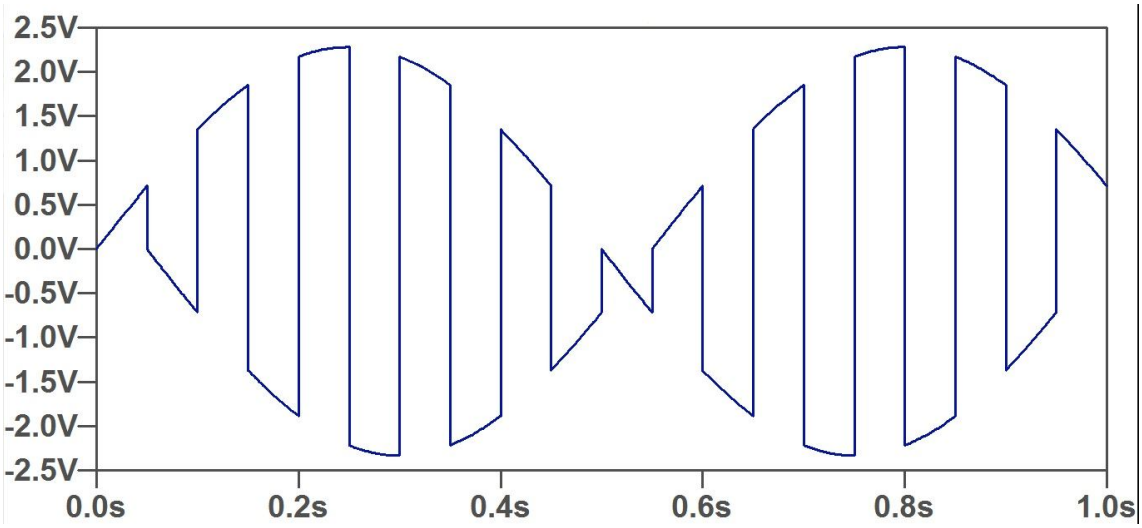

Fig. ٥-٣ SPICE simulation for pre-modulated sinusoidal input signal with ١ Hz frequency

٥.٢ PROPOSED LEAD PWM CIRCUIT

Memristor behaviour can be related to PWM by means of a comparator that compares the voltage level across the memristor with a reference voltage to give the appropriate output. Figure ٥-٤, shows a basic postulation for lead PWM circuit.

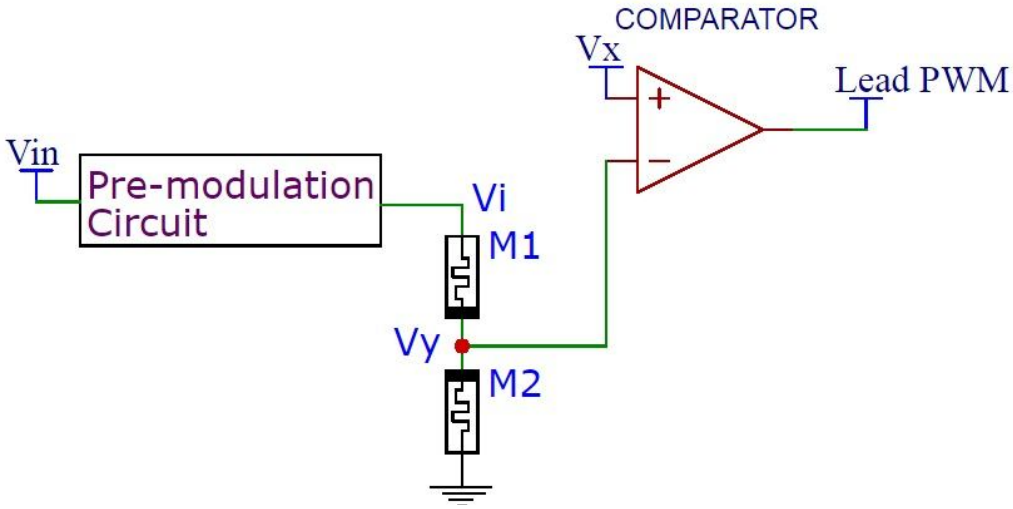

Fig. ٥-٤ Proposed lead PWM circuit diagram

٥.٢.١ Circuit operation

To understand the operation of the proposed circuit, the sampled input period is divided into two phases; the evaluation phase, which represents the first half of the sampled input period where the sampled signal is positive, and the resetting phase, which represents the second half of the sampled input period where the negative of the sampled signal exists.

The pre-modulated input signal Vi supplies a voltage divider circuit consists of two memristors; M١ and M٢. The output of the divider circuit; Vy is compared to a fixed voltage Vx. During the evaluation phase, the voltage drop across M٢; Vy is initially higher than the reference voltage Vx. So, the negative terminal of the comparator is at higher voltage. Hence, the output of the comparator is low. The memristance M١ starts to decrease and so as the voltage drop across it until the voltage drop reaches Vx which causes the negative terminal of the comparator to be in a lower voltage level, hence the output becomes high. The output comparator pulse duration depends on the speed at which the voltage drop across the memristor M٢ reaches Vx. The voltage Vx in return depends mainly on the input voltage level. From studying the linear model of the memristor, it's clear that higher voltage drop across the memristor corresponds to higher changing rate and this is the basic idea for the PWM design. During the resetting phase, the voltage Vx is now negative, so the output of the comparator will be high throughout this phase.

٥.٢.٢ Mathematical analysis

The memristor behaviour equation of two identical series-connected memristors with opposite polarities was derived on [٦], the memristance can be obtained by

$$R_{M٢}(t) = R_{ini٢} - \frac{k'_٢ \phi(t)}{R_{ini١} + R_{ini٢}} \qquad (٥\text{-}١)$$

Where $R_{ini١}$ and $R_{ini٢}$ are the initial resistances of M١ and M٢ respectively, $\phi(t)$ is the flux of the input voltage to the network and $k'_٢ = \frac{\mu_v R_{on}(R_{off} - R_{on})}{D^٢}$ which depends on the mobility factor$\mu_v(m^٢ s^{-١} V^{-١})$, R_{on} is the minimum resistance, R_{off} is the maximum resistance and D is the memristor length. As the voltage is constant during evaluation phase then

$$R_{M٢}(t) = R_{ini٢} - \frac{k'_٢ V_i T_o}{\epsilon} \qquad (٥\text{-}٢)$$

Where $\epsilon = R_{ini١} + R_{ini٢}$ is constant for identical opposite memristors.

The voltage divider across the memristor is

$$V_y(t) = \frac{V_i R_{M٢}(t)}{\epsilon} \qquad (٥\text{-}٣)$$

Note that the comparator will switch when $V_y = V_x$ as shown in Fig. ٥-٥ which enforces the output to high.

By interchanging V_y by V_x and substituting from (٥-٢) into (٥-٣) and solving for T_o the result becomes

$$T_x = \left(\frac{R_{ini٢}}{V_i \epsilon} - \frac{V_x}{V_i^٢}\right) \frac{\epsilon^٢}{k'_٢} \qquad (٥\text{-}٤)$$

The total output duration will be as follows

$$T_d = T_s - T_x \qquad (٥\text{-}٥)$$

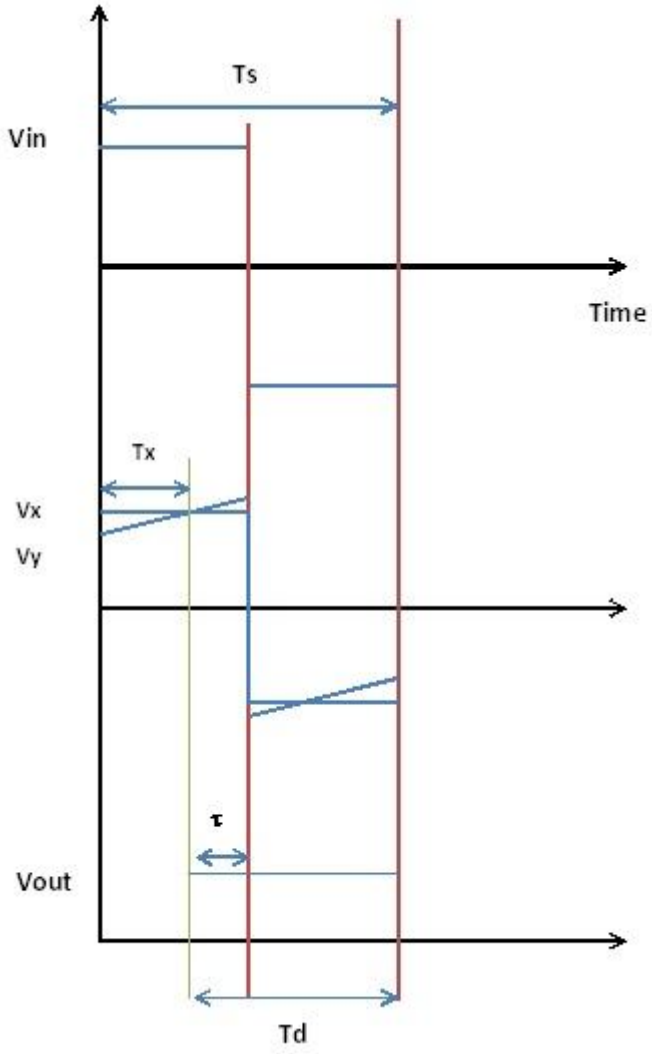

Fig. ٥-٥ Mathematical analysis for one time duration of the lead PWM

For proper operation the sufficient condition that would maintain time to be positive in (٥-٤) can be found as

$$\frac{R_{ini}{}^{٢}}{V_i \epsilon} > \frac{V_x}{V_i^{٢}} \qquad (٥\text{-}٦)$$

From which it's deduced that

$$V_x < \frac{V_i R_{ini}{}^{٢}}{\epsilon} \qquad (٥\text{-}٧)$$

Another condition for proper operation would be the value of V_x that would guarantee a proportional relation between time and V_y or mathematically

$$\frac{\partial T_d}{\partial V_i} > ٠ \qquad (٥\text{-}٨)$$

Differentiating (٥-٤) with respect to V_i and substituting into (٥-٨) forV_x, the condition becomes

$$V_x < \frac{V_i R_{ini}{}^{٢}}{{}^{٢}\epsilon} \qquad (٥\text{-}٩)$$

Combining the two conditions from (٥-٧) and (٥-٩), the sufficient condition on the reference voltage V_x over the range of the input signal will be

$$V_x < \frac{R_{ini}{}^{٢}}{{}^{٢}\epsilon} \min\,(V_i) \qquad (٥\text{-}١٠)$$

The condition for sampling time must guarantee the work within time boundaries. Using the evaluation phase duration, it can be stated that

$$T_x < \frac{T_s}{٢} \qquad (٥\text{-}١١)$$

Substituting from (٥-٤) into (٥-١١) and solving for T_s

$$T_s < \frac{{}^{٢}\epsilon R_{ini}{}^{٢}}{K_{٢}'} \min\,(\frac{١}{V_i}) \qquad (٥\text{-}١٢)$$

Therefore, the necessary and sufficient conditions for proper operation are summarized by (٥-١٠) and (٥-١٢).

٥.٢.٣ Results and simulation

SPICE simulations for the proposed PWM circuit are performed using Biolek model [٨] for memristor with$R_{on} = ١٠٠\Omega,\ R_{off} = ١٦K\Omega,\ R_{ini} = ٦K\Omega,\ D = ١٠Nm,\ \mu_v = ١٠f,$ $p = ١٠$. Whereμ_v is the mobility of the memristor and p is the doping factor.The calculatedK' equals $١٥٩M$. Figure (٥-٦) shows the theoretical value of T_d versus the input voltage for different values ofV_x.

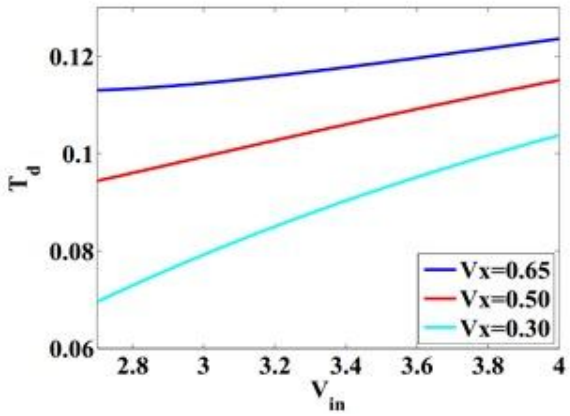

Fig. ٥-٦ Output duration versus input voltage for different V_x

These results are calculated by substituting first into (٥-٤) and (٥-١٠) and selecting$V_x = ٠.٦V$. For example, the theoretical results show $T_x = ٧٦.٤ms$ at $V_{in} = ٤V$ and $T_x = ٧١.٥ms$ at$V_{in} = ٤.٥V$. Figure (٥-٧) shows the SPICE simulation results for the same input samples with Biolek memristor model with the same parameters and it's obvious that the simulation matches the expected results with almost no error.

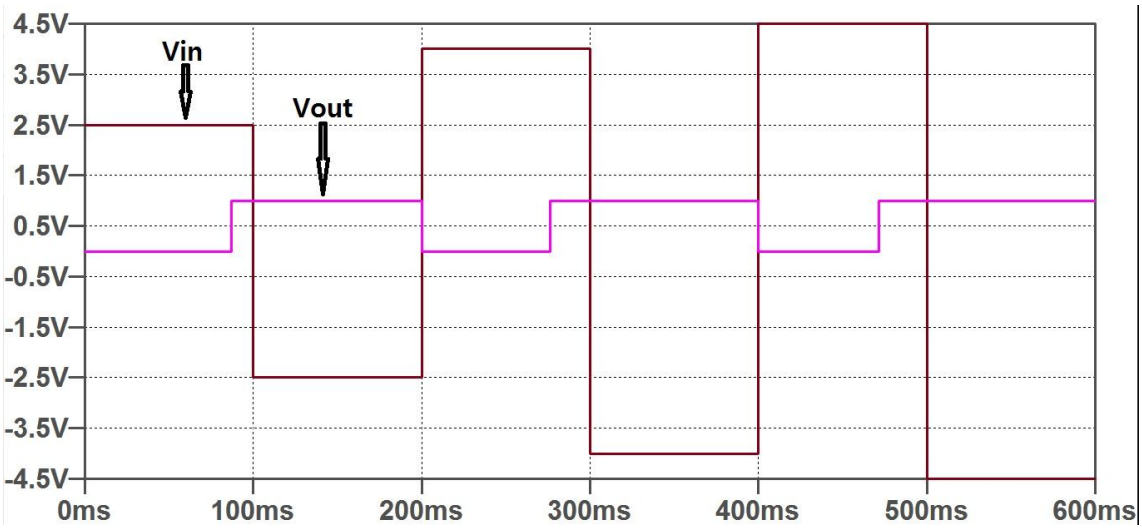

Fig ٥-٧ SPICE simulation for the lead PWM

٥.٣ PROPOSED TAIL EDGE PWM CIRCUIT

Just as the lead edge PWM, the same analysis and the same results hold except this time, it's desired to obtain a trail PWM output. Figure (٥-٨) shows the circuit diagram for the proposed trail PWM circuit.

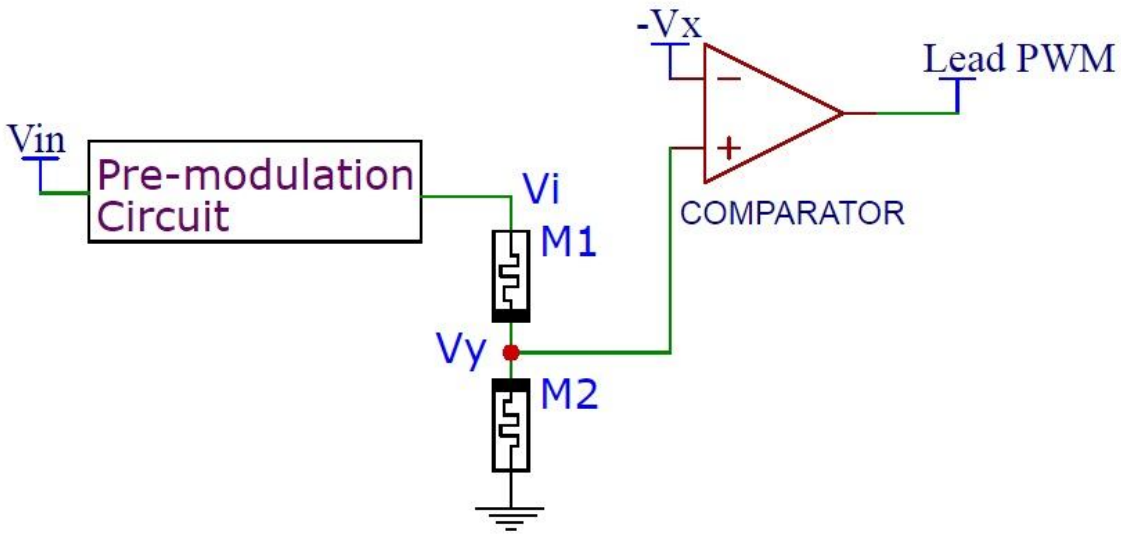

Fig. ٥-٨ proposed trail PWM circuit diagram

This can be obtained byreversing the polarity of the comparator and the voltageV_x. So, the output of thecomparator maintains high during whole evaluation phase and drops to low in theresetting phase when the drop across the memristor reachesV_x. Figure(٥-٩), shows the SPICEsimulation output for the same parameters used in the last discussion in Section ٥.٢.٣.

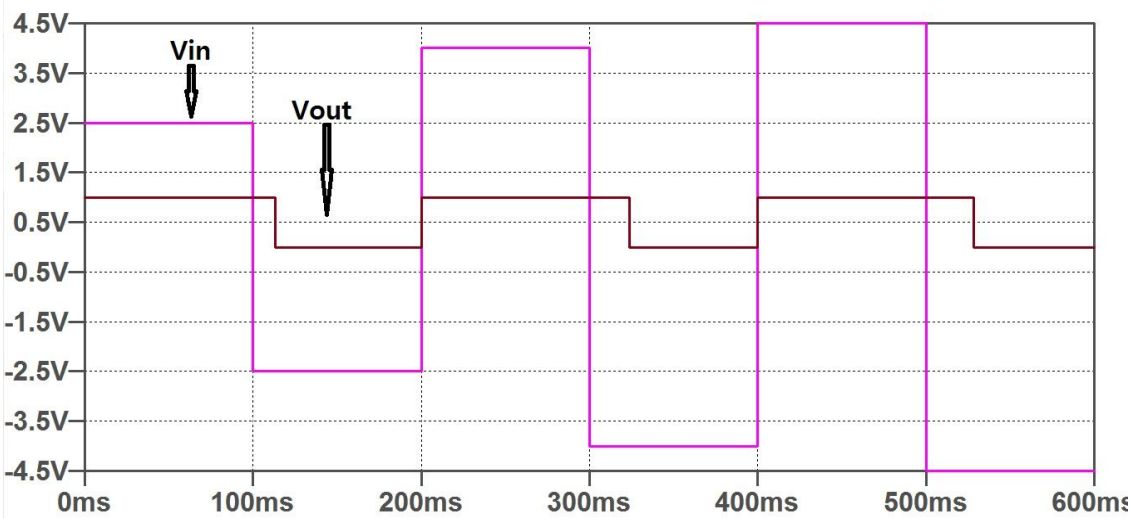

Fig. ٥-٩ SPICE simulation results for the trail PWM circuit

٥.٤ CENTRE PWM

٥.٤.١ Basic concept

In fact, the lead and trail designs have essential drawback of the power consumption as the output is always high in resetting phase in lead design and the same thing for the trail design in the evaluation phase, which is basically a waste in bandwidth which in return decreases the efficiency of the circuit in both cases. Therefore, here comes the need for the centre PWM technique. Assume using same memristors in both designs (Lead PWM and Trail PWM) and using the same reference voltage V_x with opposite polarities, the centre PWM can be obtained by simply ANDing the two outputs of the Lead and Trail PWM circuits (i.e. pass the two outputs by an AND gate). Figure ٥-١٠, shows the basic circuit diagram for the proposed centre PWM circuit.

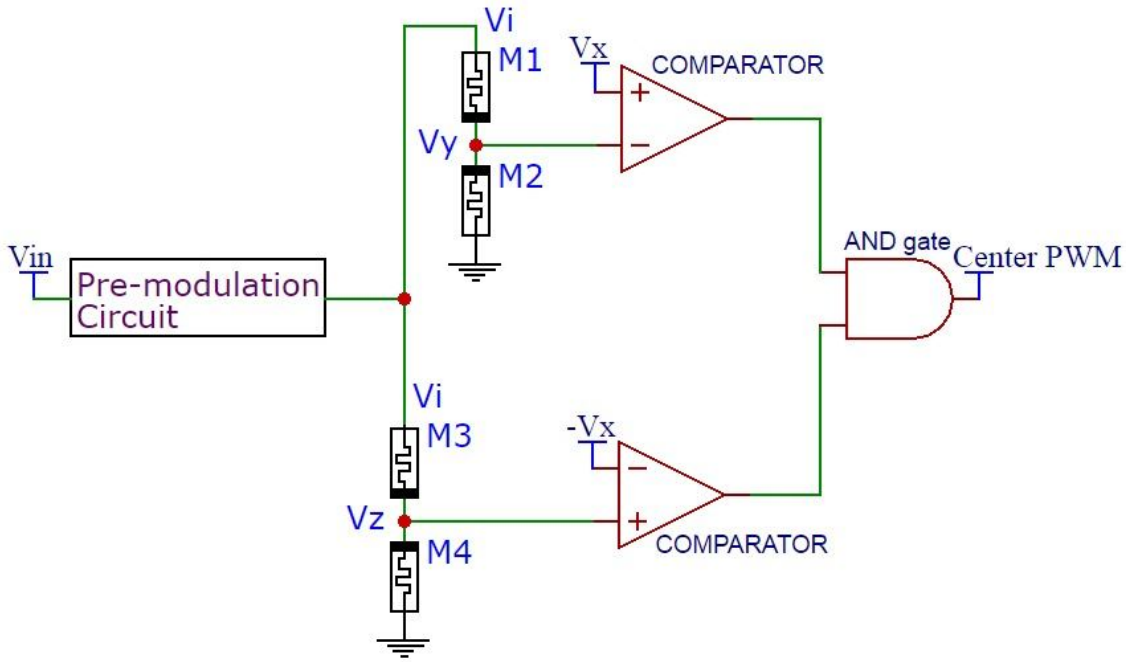

Fig. ٥-١٠ proposed center PWM circuit diagram

٥.٤.٢ Mathematical analysis and simulation results

Same procedure that followed in the lead edge PWM could be carried out to get the output time duration of the proposed centre PWM circuit. The output time duration is derived to be as follows

$$T_d = T_s - ٢T_x \qquad (٥\text{-}١٣)$$

Since the proposed centre PWM circuit is designed using lead edge and trail edge proposed circuits as building blocks, then, the same conditions in (٥-١٠) and (٥-١٢) apply. By substitution from (٥-٤) into (٥-١٣), the output centre PWM duration becomes

$$T_d = T_s + \left(\frac{V_x}{V_i^2} - \frac{R_{ini^2}}{V_i \epsilon}\right)\frac{2\epsilon^2}{k_2'} \qquad (٥\text{-}١٤)$$

Figure ٥-١١, shows the theoretical value of Td versus the input voltage for different sampling time values.

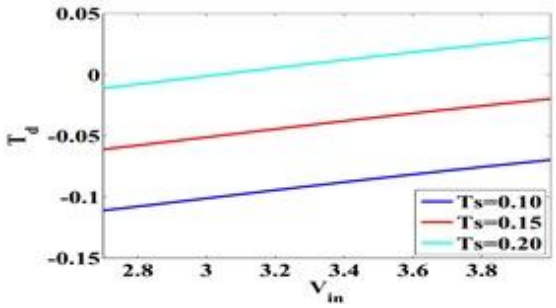

Fig. ٥-١١ Output duration versus input voltage for different T_S

Using the same theoretical example that was used in lead PWM with three different input levels and sample time is $٢٠٠ms$, the output duration is $T_d = ٢٦.٢ms$ for$V_{in} = ٢.٥V$, $T_d = ٤٧.٢ms$ for $V_{in} = ٤V$ and $T_d = ٥٦.٨٨ms$ for$V_{in} = ٤.٥V$. The PSPICE simulation results for the proposed centre PWM circuit are shown in (٥-١٢). The simulation results show a great match to the theoretical results with almost no error.

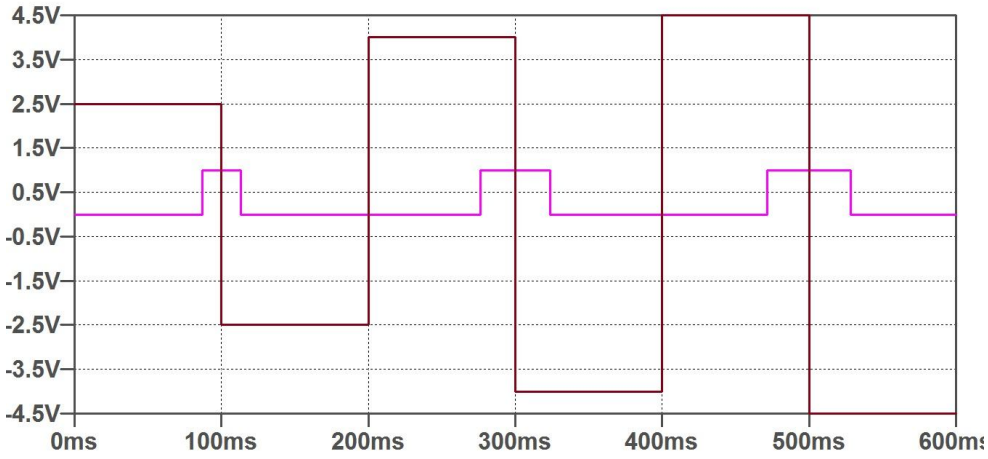

Fig. ٥-١٢ SPICE simulation results for the center PWM circuit

٥.٥ ADDITIONAL CENTER PWM DESIGN

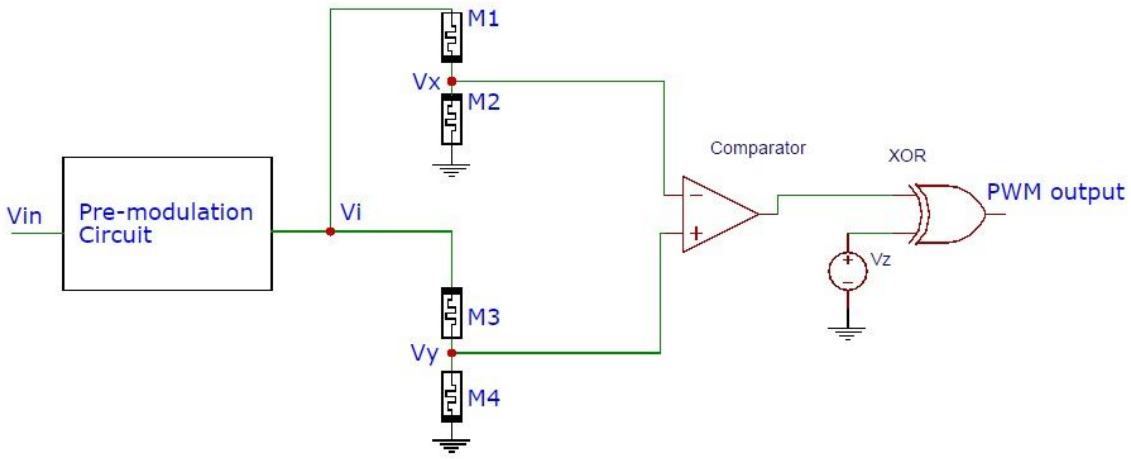

Fig. ٥-١٣ Center PWM additional design

The operation is the same as the preceding circuit provided that the initialmemristance of the upper network divider be greater than that of the lower to ensure that V_x is initially greater than V_y

$$R_{ini٢} > R_{ini٤} \qquad (٥\text{-}١٥)$$

Initially M٤ will have lower voltage drop than M٢ which will lead the comparator to have low output. As time passes, M٤ is increasing and M٢ is decreasinguntil they have the same voltage drop after T_x time which will lead the comparator to have high output. During the second half of the input sample duration, thereverse will happen therefore, an XOR with$V_z$having the same input sample duration will ensure to maintain the output at the first half of the sample durationand reverse it in the second half.

٥.٥.١ Mathematical analysis

The aim is to computeT_x as indicated in Fig. ٥-١٤. Once computed,T_d(theoutput pulse width duration) can be easily evaluated.

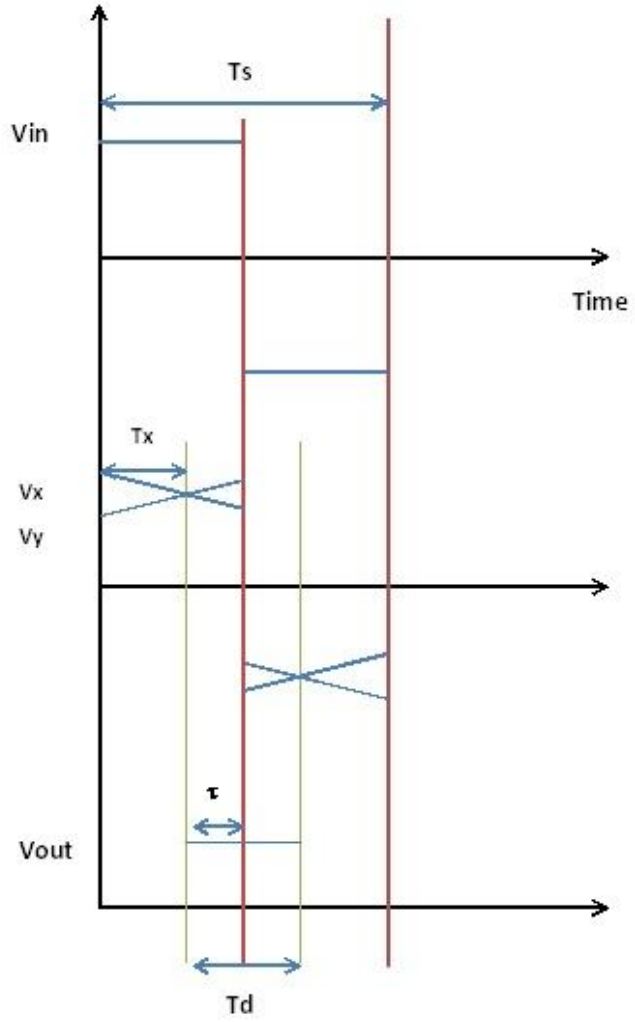

Fig. ٥-١٤ one input sample analysis for the center PWM additional design

Starting with the upper network, the voltage divider across the network is

$$V_x = V_i \frac{R_{M٢}}{R_{M١}+R_{M٢}} \qquad (٥\text{-}١٦)$$

It should be noted that M١ and M٢ are connected with opposite polaritiestherefore, if they are identical

$$R_{M١} + R_{M٢} = \epsilon_١ = R_{in_{M١}} + R_{in_{M٢}} \qquad (٥\text{-}١٧)$$

Where$\epsilon_١$ is constant.

Same result is achieved with the down network

$$V_y = V_i \frac{R_{M٤}}{R_{M٣}+R_{M٤}} \qquad (٥\text{-}١٨)$$

$$R_{M٣} + R_{M٤} = \epsilon_٢ = R_{in_{M٣}} + R_{in_{M٤}} \qquad (٥\text{-}١٩)$$

From Fig. ٥-١٤, T_x is the duration until the two voltage drops become equal, therefore

$$V_x = V_y \qquad (٥\text{-}٢٠)$$

Substituting from (٥-١٦) - (٥-١٨) into (٥-٢٠)

$$\frac{R_{M٢}}{R_{M١}+R_{M٢}} = \frac{R_{M٤}}{R_{M٣}+R_{M٤}} \qquad (٥\text{-}٢١)$$

Now substituting from (٥-٣) for$R_{M٢}$and $R_{M٤}$ in (٥-٢١)

$$R_{in_{M٢}} - \frac{K'_٢}{R_{in_{M١}}+R_{in_{M٢}}}\phi(t) =$$

$$\left(\frac{R_{in_{M١}}+R_{in_{M٢}}}{R_{in_{M٣}}+R_{in_{M٤}}}\right)\left(R_{in_{M٤}} - \frac{K'_٤}{R_{in_{M٣}}+R_{in_{M٤}}}\phi(t)\right) \qquad (٥\text{-}٢٢)$$

Where $\phi(t)$ is the time integral of the input voltageV_i.

Substituting for the flux by its integral equivalence and from (٥-١٧) and (٥-١٩) all into (٥-٢٢)

$$R_{in_{M٢}} - \frac{K'_٢ V_i T_x}{\epsilon_١} = \left(\frac{\epsilon_١}{\epsilon_٢}\right)\left(R_{in_{M٤}} - \frac{K'_٤ V_i T_x}{\epsilon_٢}\right) \qquad (٥\text{-}٢٣)$$

Rearranging for T_x

$$V_i T_x \left(\frac{K'_٢}{\epsilon_١} - \frac{K'_٤ \epsilon_١}{\epsilon_٢^{٢}}\right) = \left(R_{in_{M٢}} - \frac{\epsilon_١}{\epsilon_٢} R_{in_{M٤}}\right) \qquad (٥\text{-}٢٤)$$

Up to this point, assuming that M٢ and M٤ have the same mobility and physical structure, therefore

$$K'_٢ = K'_٤ = K = \frac{\mu_v R_{on}(R_{off}-R_{on})}{D^{٢}} \qquad (٥\text{-}٢٥)$$

Note the negative sign of$K'_٤$is due to the reverse polarity of M٤.

Considering (٥-٢٥), solving (٥-٢٤) for T_x will lead to

$$T_x = \frac{١}{V_i K}\left(\epsilon_٢ R_{in_{M٢}} - \epsilon_١ R_{in_{M٤}}\right)\left(\frac{\epsilon_١ \epsilon_٢}{\epsilon_١^{٢} + \epsilon_٢^{٢}}\right) \qquad (٥\text{-}٢٦)$$

Substituting from (٥-٢٦) into (٥-١٣), the output duration turns out to be

$$T_d = T_s - T_x = \frac{٢}{V_i K}\left(\epsilon_٢ R_{in_{M٢}} - \epsilon_١ R_{in_{M٤}}\right)\left(\frac{\epsilon_١ \epsilon_٢}{\epsilon_١^{٢} + \epsilon_٢^{٢}}\right) \qquad (٥\text{-}٢٧)$$

WhereT_S is the input sample duration.

٥.٥.٢ Results and simulation

Using physically identical memristors with$\mu_v = ١٠ fm^{٢} s^{-١} V^{-١}$, $D = ١٠ nm$,$R_{off} = ١٦ k\Omega$ and $R_{on} = ١٠٠\Omega$. This corresponds to $K = ١٥٩ M\Omega^{٢} s^{-١} V^{-١}$. Setting initial resistances as$R_{in_{M١}} = R_{in_{M٤}} = ٠.٥ K\Omega$ and$R_{in_{M٢}} = R_{in_{M٣}} = ٦ K\Omega$ and using input voltage with$T_s = ٢٠٠ ms$ period duration, T_x is computed from (٥-٢٦) for three different input samples; the results are

- $T_x = ٧٤.٩٤ ms$ for $V_{in} = ١.٥ V$, therefore,$T_d = ٥٠.١٢ ms$
- $T_x = ٤٤.٩٦٨ ms$ for $V_{in} = ٢.٥ V$, therefore,$T_d = ١١٠.٠٦٤ ms$
- $T_x = ٢٨.١٠٥ ms$ for $V_{in} = ٤ V$, therefore,$T_d = ١٤٣.٧٩ ms$

Figure ٥-١٥ shows the SPICE simulation for the memristor-based PWM circuit for three input different samples with ٢٠٠ms duration. The results match the theoretical analysis with almost no error.

Fig. ٥-١٥ center PWM SPICE simulation for three input samples with different levels

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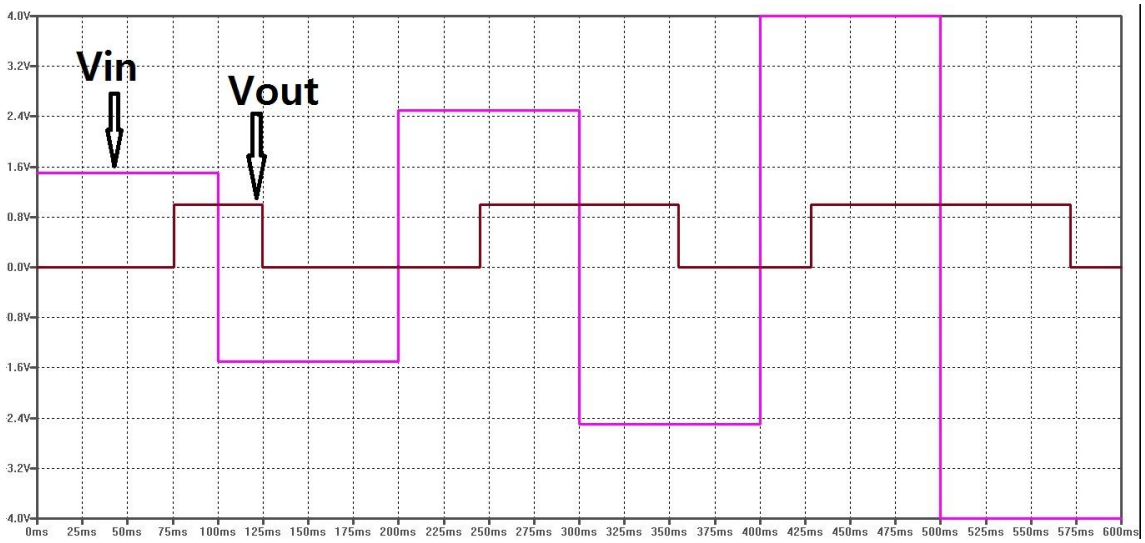

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