Fayoum University
Faculty of Engineering
Electrical Engineering Dep.

Electronics 3 (ECE301)
Final Term Exam
09/01/2016

-Time allowed: 3 hours **-Maximum degree: 90** **-Attempt all the 7 questions**

Problem (1) [10 pts]:

A basic two quadrant multiplier is shown in Fig.1. All transistors are assumed matched.

(a) Find the relation between $I_{out} = (I_1 - I_2)$ and the inputs ΔI_X and I_Y.

(b) Design the circuit needed to obtain a differential output current from an input voltage V_X, and the circuit needed to obtain an output current I_Y from an input voltage V_Y.

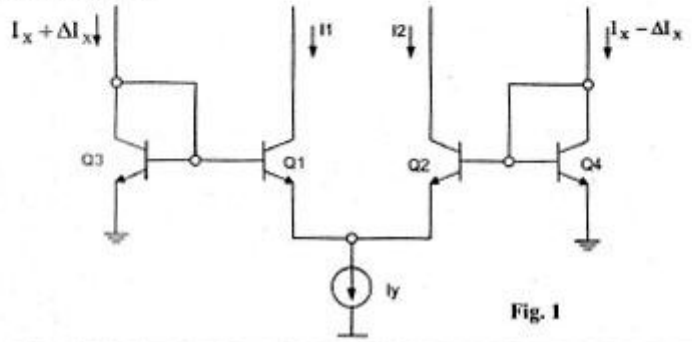

Fig. 1

Problem (2) [15 pts]:

(a) For the level shifter circuit shown in Fig. 2(a), assuming M_a and M_b are matched and operating in the saturation region, **show that:** $V_b = V_1 - V_{C1} + V_{C2}$.

(b) The level shifter in prob. 2(a) is used in the circuit shown in Fig. 2(b) to implement MOS multiplier. **Show that:** $I_{out} = I_a - I_b = K(V_{C1} - V_{C2})(V_1 - V_2)$, where K is the transconductance parameter of the transistors M_1, M_2, M_3, and M_4.

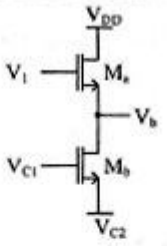

Fig. 2(a)

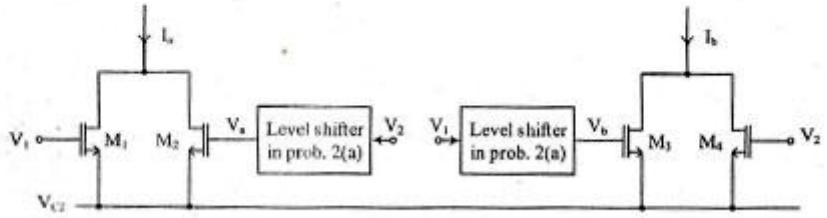

Fig. 2(b)

Problem (3) [10 pts]:

A log-antilog analog multiplier is shown in Fig. 3. The output voltage V_o is a function of the product of two inputs V_x and V_y.

(a) Find the relation between the output V_o and the input voltages V_x, V_y, and V_r.

(b) What are the limitations on V_x and V_y? How many Quadrants obtained?

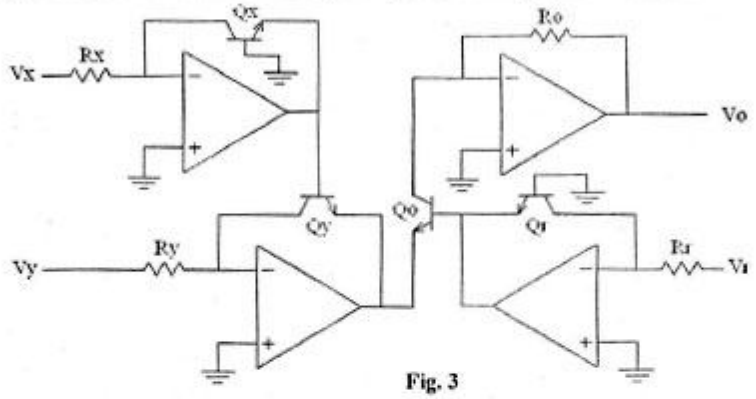

Fig. 3

Problem (4) [15 pts]: An Asymmetrical SQW generator is shown below, where V_P is a constant D.C. voltage of 2V. The zener diodes are assumed ideal with V_Z=6V and V_{Don}=0V.

(a) Sketch the output voltage waveform and the capacitor voltage waveform.

(b) Find the frequency of the free running circuit.

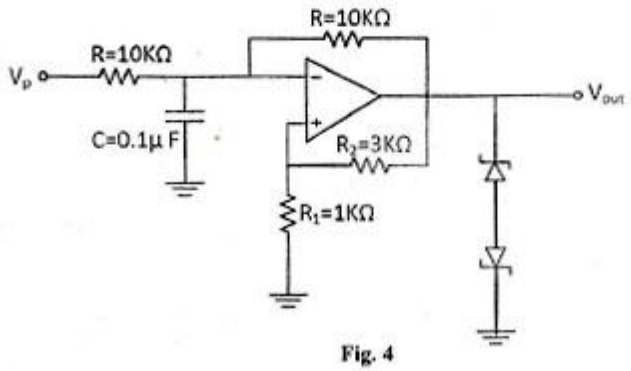

Fig. 4

Problem (5) [15 pts]: For the TTL logic gate shown in Fig. 5, β_F =200 and β_R =2 for the NPN transistors Q_1 and Q_3, while β_F =30 and β_R =3 for the PNP transistor Q_2:

(a) Calculate V_{OH} and V_{OL}.
(b) What is the average static power consumption? (assuming 50% duty cycle)
(c) What are the input currents in the two logic states?
(d) What is the fan out capability of the gate?
(e) What is the logic function of the gate?

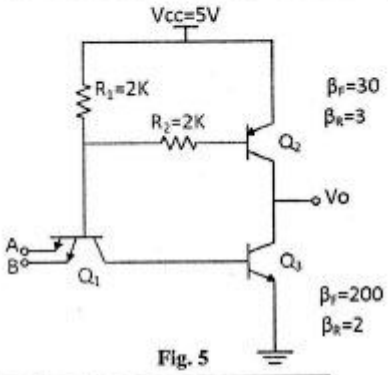

Fig. 5

Problem (6) [15 pts]: Consider the enhancement-load inverter shown in Fig. 6. V_{T0}=1V, $(W/L)_1$=4, $(W/L)_2$=1/4, $\mu_n C_{ox}$=20μA/V² and V_{DD}=5V.

(a) Sketch the VTC of the inverter showing the mode of operation for M_1 in each region.
(b) Find V_{OH}, V_{OL}, V_{IH}, V_{IL} and hence find NM_H and NM_L.
(c) Find the static power dissipation
(d) Find the current available for discharging a load capacitor when V_I=V_{OH} and V_O=4V and 1V.
(e) Realize the following function: F=(A+B)(C+D)

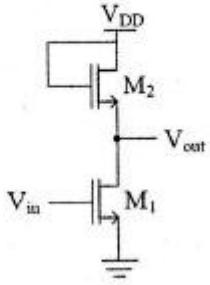

Fig. 6

Problem (7) [10 pts]:

Design a 3-bit folded resistor-string D/A converter. Use 2 to 1-of-4 decoder with the most significant two bits (b_1b_2) to decode word lines, and use 1 to 1-of-2 decoder with the least significant bit (b_3) to decode bit lines. Clearly show your transistor connections.

Best Wishes!

Dr. Mohammed A. Hassan