Design Interconnect Network Between Dual Core RISC_V Processor Opensource

A Thesis Submitted in Partial Fulfillment of the Requirement for the Degree of Master of Science

In

Electrical Engineering Department

Electronics and Communications Engineering

Introduced By:

Eng. Demyana Emil Mekhail Selim

Under Supervision:

Assoc. Prof. Dr. Gihan Nagib Abd-El Sattar Negm

Associate professor, Electrical Engineering Department

Faculty of Engineering, Fayoum University

(Main Supervisor)

Dr. Mohammed Hamdy Mohammed Abd-Ellah Merzaban

Assistant professor, Electrical Engineering Department

Faculty of Engineering, Fayoum University

(Co-Supervisor)

Faculty of Engineering, Fayoum University

Fayoum, Egypt

2023

ABSTRACT

Multi-core RISC-V processors have a promising impact in the digital computing design area. They offer several benefits, especially in performance. Additionally, the RISC-V architecture set is open-source so researchers can build and enhance computing systems. Unfortunately, there are few open-source multiprocessor RISC-V. Therefore, in this thesis, an open multi-core RISC-V processor is implemented. Its design is based on an open-source single RvCore processor (Taiga). Two cores of Taiga are integrated on-chip. The thesis addresses various Synthesis topics, such as cache coherence, interconnection, memory structure problems, and availability of customized peripheral devices. To achieve data coherence between implemented caches and the main memory, a solution based on the snoopy protocol has been developed. A hardware-customized peripheral unit has also been developed to manage work and halt cases among working cores, while another peripheral unit has been implemented for communication with another processor or PC using the UART protocol. An AXI-interconnect has been implemented to connect the cores with the customized peripheral devices. This interconnection depends on the multiplexer structure. It interfaces with the cores via the AXI protocol. Each peripheral device has a specific address (port number) according to the address mapping concept. Some modules (memory unit) of the design have been redesigned to make the design synthesizable on the FPGA family. Finally, extensive testing and benchmarks were conducted to assure correct functionality and good performance. The system performance has been assessed using standard multi-core benchmarks (CoreMark) and other developed benchmarks on Zedboard (Xilinx FPGA). The two cores can operate independently or dependently. Dependently, a specific task is distributed on the two cores and the first core (that finished its task first) waits for the other. Independently, each core operates individually. The improvement percentage of the multiprocessor's performance varies. For example, in the case of CoreMark testing, the dual-processor achieved 4.605 CoreMark/MHz with an operating frequency of 98 MHz. In 100-numbers summed (dependent tasks), the dual-processor has executed the program in 914 clock cycles with an operating frequency of 10 MHz which is 21.05% better than that achieved by a single processor (1158 clk) with the same operating frequency. The improvement percentage of the multiprocessor’s performance varies depending on the program's complexity. The maximum operating frequency of the processor is 98 MHz.