



Cairo University

A LOW-POWER 64GB/S PAM4 TRANSMITTER IN 65NM CMOS

By

Yasmeen Tantawy

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE
in
Electronics and Communications Engineering

FACULTY OF ENGINEERING, CAIRO UNIVERSITY
GIZA, EGYPT
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Summary:

This research presents a PAM4 transmitter design operating at 64 Gb/s using 65nm CMOS technology, achieving high energy efficiency of 0.95 pJ/bit and total power consumption of 60.8 mW. The design relies on a three-stage serializer that includes a transmission-gate-based multiplexer, a charge-steering multiplexer, and a 4:1 multiplexer using Current-Mode Logic (CML). This architecture achieves an optimal balance between speed and power, with an output swing of 1.14 VPP and a high linearity level (RLM) of 98.3%.

The study addresses key design challenges, such as signal integration, signal termination, delay management, and precise timing control. Advanced techniques are introduced to improve signal integrity, reduce noise, and minimize timing issues between bits with varying weights. The design achieves a horizontal eye opening of 0.83 UI, ensuring accurate data recovery for high-speed communication systems.

Key Words:

PAM4 , SST, 4:1 MUX, CML to CMOS, charge-steering mux, CMOS MUX