Ali M.K., Hamidian A., Malignaggi A., and Boeck G., "Utilizing Static Frequency Divider for Quadrature Signal Generation in a 90 nm CMOS Technology," in Microwave Conference (GeMIC), Germany, vol.1, no.4, pp. 10-12, March 2014

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Abstract: This work presents a design of a static frequency divider (SFD). Purpose of the divider is to generate quadrature signals at half the input frequency. Power consumption considerations are taken into account. The SFD-IQ generator is realized in a 90 nm CMOS technology with a chip area of 0.60??0.75 mm(exp 2). It self-oscillates at 20.5 GHz and has a locking range of 12 GHz. The output power is more than -16 dBm and the input sensitivity is-1 dBm. The SFD core power consumption is 6.9 mW from a 1.2 V power supply, which is the lowest value reported. The IQ imbalance and the corresponding image rejection ratio (IRR) are mathematically modeled, simulated and measured. Imbalance of output phase and amplitude are 2deg and 0.7 dB respectively, while the IRR is around 29 dB.