Interconnection Mechanism For Multi-Core Architectures With Shared Cache Memory

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Abstract

This paper addresses the interconnection design issues of area, power and performance of chip multi processors with shared cache memory. It shows that having shared cache memory contributes a lot to an improved performance, but typical interconnection between cores and the shared cache using crossbar occupies most of the chip area and consumes a lot of power and also does not scale efficiently with increased number of cores. New interconnection mechanisms are needed to address these issues. This research suggests an architectural paradigm in an attempt to gain the advantages of having shared cache with the avoidance of penalty imposed by the crossbar interconnect. The proposed architecture achieves smaller area occupation allowing more space to add additional cache memory. It also achieves better power consumption compared to the existing crossbar architecture (about 60% of the power consumed by the crossbar).

Keywords: *Chip Multi Processors, Shared cache memory, Interconnection mechanisms*

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References

1. Zvika G., Idit K., Avinoam K., and Uri W., "Nahalal: Cache Organization for Chip Multiprocessors," IEEE Computer Architecture Letters, Vol. 6, No. 1, pp. 21-24, 2007.
2. Rakesh Kumar: "Holistic Design for Multi-core Architectures",PhD thesis, University of California, San Diego, 2006
3. Terry Tao Ye, "On Chip Multiprocessor Communication Network Design and Analysis", PhD thesis, Stanford university, 2003
4. A. Hemani, A. Jantsch, S. Kumar, A. Postula, J. Oberg, M. Millberg, D. Lindqvist, ”Network on a Chip: An architecture for billion transistor era”, In Proceeding of the IEEE NorChip Conference, pp.166-173 2000.
5. L. Hammond, B. A. Nayfeh, and K. Olukotun. "A single-chip multiprocessor". IEEE Computer, Vol. 30, No. 9, pp. 2-11, 1997.
6. Jaehyuk Huh, Changkyu Kim, Hazim Shafi, Lixin Zhang, Doug Burger, and Stephen W. Keckler, "A NUCA Substrate for Flexible CMP Cache Sharing," IEEE Transactions on Parallel and Distributed Systems, Vol. 18, No. 8, pp. 1028-1040, 2007

7. Terry Tao Ye and Giovanni De Micheli, "Physical Planning for On-Chip Multiprocessor Networks and Switch Fabrics," In Proceeding of the14th IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP'03), pp. 97-107, 2003
8. Cidon I. and Keidar I.: "Zooming in on Network on Chip Architectures", Technical Report CCIT 565, Technion Department of Electrical Engineering, Israel Institute of Technology, 2005
9. Frank S. J. "Tightly coupled multiprocessor systems speed memory access times". In Electron, Vol. 57, pp. 164-169, 1984.
10. Lovett T. and Thakkar S. "The symmetry multiprocessor system". In the Proceedings of the International Conference on Parallel Processing ICPP '88, The Pennsylvania State University, University Park, Vol. 1, pp. 303-310, 1988.
11. Wilson A. "Hierarchical cache/bus architecture for shared memory multiprocessors", Proceedings of the 14th annual international symposium on Computer architecture, pp. 244-252, Pittsburgh, Pennsylvania, United States1987 .
12. James Archibald and Jean-Loup Baer. "Cache coherence protocols: evaluation using a multiprocessor simulation model", ACM Transactions on Computer Systems (TOCS), Vol. 4, pp. 273-298, 1986.
13. Ho R., Mai K., and Horowitz M., "The future of wires," Proceedings of IEEE, Vol. 89, issue 4, pp. 490-504, 2001.
14. Howard E., "Garden Cities of To-Morrow," London: Swan Sonnenschein & Co. Ltd, 1902
15. Dally W. J., "A VLSI Architecture for Concurrent Data Structures", Kluwer Academic Publishers, Norwell, MA, USA, 1987.
16. Bolotin E., Cidon I., Ginosar R. and Kolodny A.: "QNoC: QoS architecture and design process for Network on Chip", Journal of Systems Architecture: the EUROMICRO Journal, Vol. 50 , Issue 2-3, pp. 105-128, 2004